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IN THIS ISSUE

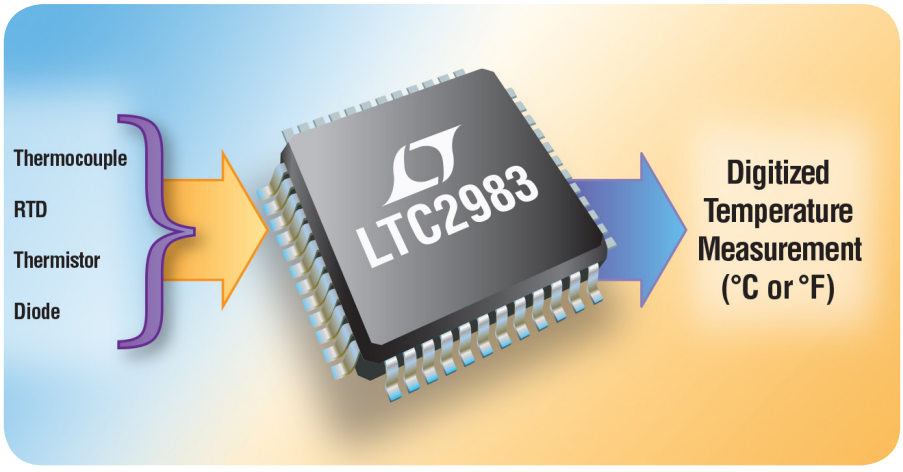
Temperature-to-Bits: One IC for All Sensor Types, 0.1°C Conformity

Michael Mayes

Temperature measurement is not new. Galileo invented a rudimentary thermometer capable of detecting temperature changes, and two hundred years later, Seebeck discovered the thermocouple. Given the long history of temperature measurement and its extensive use today, one would think that accuracy problems were all but eliminated. Not so. Even though methods for extracting temperature from sensor elements are well known, accurately measuring temperatures to better than 0.5°C or 0.1°C accuracy remains a challenge. The LTC®2983 enables up to 0.1°C temperature conformity (measured accuracy against a precision temperature calibrator), as shown in Figure 1.

Thermocouples, temperature dependent resistance elements (RTDs and thermistors) and semiconductor elements (diodes) are widely used to electrically measure temperature. Digitizing the electrical signals of these sensor elements requires significant expertise in a number of areas: sensor behavior, analog circuit design, digital circuit design and firmware development. The LTC2983 packs this expertise into a single IC and solves each of the unique challenges associated with thermocouples, RTDs, thermistors and diodes. It combines all analog circuitry necessary for each sensor type with temperature measurement algorithms and linearization data to directly measure each sensor and output the result in °C.

(continued on page 4)



The LTC2983 solves the unique problems presented by all standard temperature sensors to produce unmatched conformity and ease-of-use.

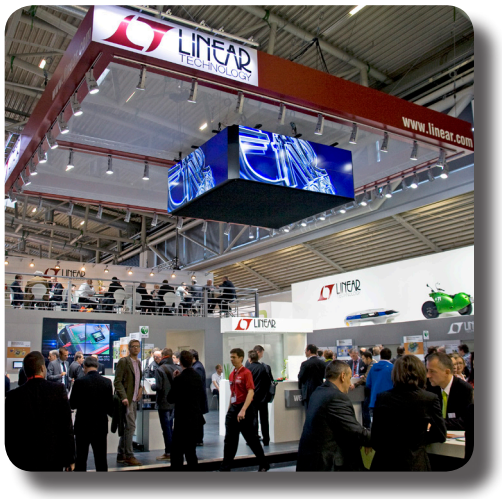
In this issue...

Linear in the News

LINEAR AT ELECTRONICA

In November, Linear had a major presence at the biannual Electronica Show in Munich. The Linear booth featured an ambitious array of 20 live, system-based demos, showcasing the breadth of the company's product line. These demos included:

- Power over Ethernet port forwarding using 90W LTPoE++™
- High performance amplifiers and converters enabling small, precise instruments
- Complete backup power—when you need it
- Maximize battery pack safety, life and capacity
- Robust IO-Link, PHY solutions
- Highly reliable wireless mesh network running on solar power
- Wireless power for battery charging in challenging environments
- Bidirectional converter allows backup power
- Precision electrocardiogram signal chain
- Solar power charging with True Maximum Power Point Tracking
- Power management for video and broadcasting
- µModule® regulator with READ/WRITE telemetry
- Universal temperature sensor IC
- E-Motorbike battery management
- Batteries of BMW i8 monitored by LTC6802 battery stack monitor



The Linear booth at Electronica was a hive of activity with 20 live system-based demos.

NEW VIDEOS

Linear has posted several new videos at www.linear.com, including:

Universal Temperature Measurement System—Michael Mayes presents a series of lab-based demonstrations that highlight the capabilities of the innovative LTC2983 universal temperature sensor IC. These TechClips show how the LTC2983 can be used to directly digitize RTDs, themocouples and thermistors to measure temperature to an accuracy of 0.1°C and report the results in °C or °F. View the TechClips at www.linear.com/solutions/5500

High Power 3-Channel LED Driver—Keith Szolusha shows how the LT®3797 powers three high power strings of LEDs with flexible topologies and major fault protection such as open LED strings and shorted LED strings. View video at www.linear.com/solutions/5466

More Power, Better Heat Dissipation, Smaller PCB Area—Video comparison of three converter options: switching controllers, monolithic regulators, and µModule regulators in terms of component count, area, design effort and thermal performance. The LTM®4633 and LTM4634 µModule regulators require the lowest component count, design effort, PCB area and address thermal concerns with an innovative package design that includes an integrated top side heat sink, creating a low thermal impedance path to the ambient air. See video at www.linear.com/solutions/5467

A Very Low Power, High Performance I/Q Modulator—This video discusses the LTC5599, a very low power modulator with excellent sideband rejection and carrier leakage suppression, and with on-chip capability to adjust these performance metrics to unprecedented levels. The device has an exceptionally low output noise floor and high linearity, producing superior dynamic range performance for mission-critical transmitters. View at www.linear.com/solutions/5429

High Efficiency Buck-Boost Battery Charger—Today's battery chargers are expected to support a variety of battery chemistries and accept a range of input voltages. In many applications, the input voltage range can vary from below the output battery voltage to above the battery voltage, requiring both step-down and step-up capability. This video shows how the LTC4020 controller meets these challenges, how it works and its main features. See the video at www.linear.com/solutions/5430

AWARDS

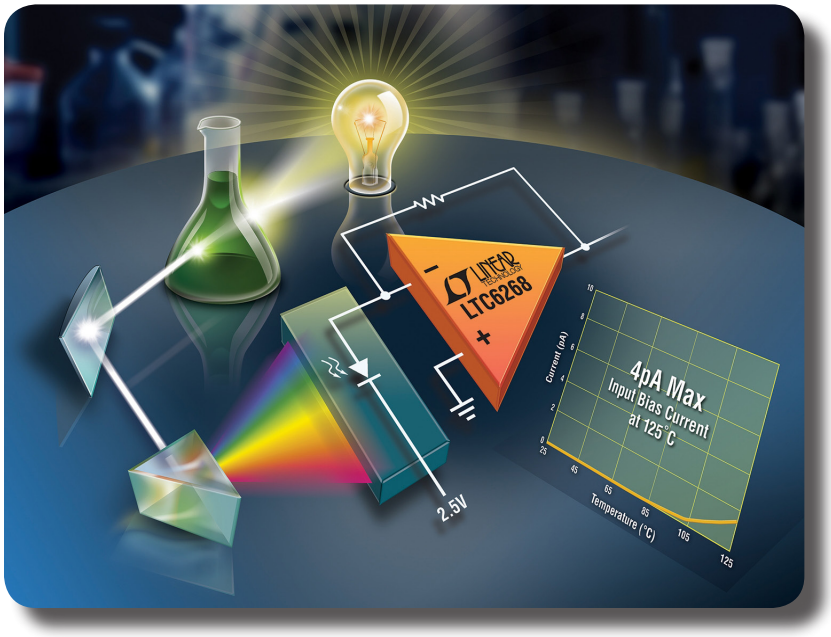
EDN Hot 100 Products for 2014

EDN in November announced the selection of several Linear Technology products as *EDN* Hot 100 Products for 2014:

- LTC6268 ultralow input bias current op amp
- LT3669 IO-Link PHY-compatible industrial transceiver
- LTC5599 direct conversion I/Q modulator

Wireless Battery Charger Selected for Two Awards

Linear's LTC4120 wireless battery charger was selected by UK's *Electronic Product Design & Test* magazine for their 2014 E-Legacy Awards in the Environmental category. The LTC4120 also brought home the award for Italy's *Selezione di Elettronica's* 2014 Innovation Award.



The LTC6268 ultralow input bias current op amp was selected as an EDN Hot 100 Product.

Linear Products Receive Awards in China

Two Linear Technology products received awards from major publications in China. The LTC2338-18 18-bit, 1Msps SAR ADC was selected by *EEPW* in their Editors' Choice Awards 2014 for Best Mixed-Signal Chip Award. And *Electronic Products China* chose the LTC3330 nanopower buck-boost converter with energy harvesting battery life extender for their Top 10 Product Award and their Green Energy Award.

CONFERENCES & EVENTS

CAR-ELE Japan, 7th International Automotive Electronics Technology Expo, Tokyo Big Sight, Tokyo, Japan, January 14-16, West 1 Hall, Booth West 8-12—Linear showcases its high performance analog IC solutions for automotive, including battery management systems. More info at www.car-ele.jp/en/Home/

APEC 2015, Applied Power Electronics Conference, Charlotte Convention Center, Charlotte, NC, March 16-18, Booth 201—Presenting Linear's broad range of power management solutions, including innovative switching regulators, linear regulators, digital power system management products and µModule regulators. Michael Jones is presenting "PMBus Firmware: Using Arduino for Prototyping and Designing PMBus Solutions" at 8:30 am, March 17. More info at www.apec-conf.org/

Electronica China, Shanghai New International Expo Centre, Shanghai, China, March 17-19, Hall E3, Booth 3318—Linear will exhibit its broad portfolio of analog and power solutions, including Silent Switcher® regulators, LDO+™ linear regulators, high power LED drivers, µModule regulators, supercap chargers, universal digital temperature measurement system, SAR ADCs, automotive battery management systems, wireless sensor network products and RF products. More info at www.electronica-productronica-china.com/en/home ■

The LTC2983 has these polynomials built in for all eight standard thermocouples (J, K, N, E, R, S, T and B) as well as user programmed table data for custom thermocouples. The LTC2983 simultaneously measures the thermocouple output and the cold junction temperature, and performs all required calculations to report the thermocouple temperature in °C.

(LTC2983, continued from page 1)

THERMOCOUPLES: OVERVIEW

Thermocouples generate voltage as a function of the temperature difference between the tip (thermocouple temperature) and the electrical connection on the circuit board (cold junction temperature). In order to determine the thermocouple temperature, an accurate measurement of the cold junction temperature is required; this is known as cold junction compensation.

The cold junction temperature is usually determined by placing a separate (non-thermocouple) temperature sensor at the cold junction. The LTC2983 allows diodes, RTDs, and thermistors to be used as cold junction sensors. In order to convert the voltage output from the thermocouple into a temperature result, a high order polynomial equation (up to 14th order) must be solved (using tables or mathematical functions) for both the measured voltage and the cold junction temperature. The LTC2983 has these polynomials built in for all eight standard thermocouples (J, K, N, E, R, S, T and B) as well as user-programmed table data for custom thermocouples. The LTC2983 simultaneously measures the thermocouple output and the cold junction temperature, and performs all required calculations to report the thermocouple temperature in °C.

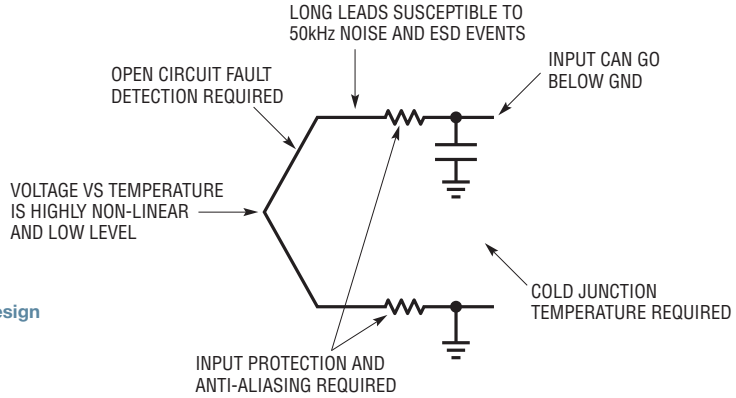


Figure 2. Thermocouple design challenges

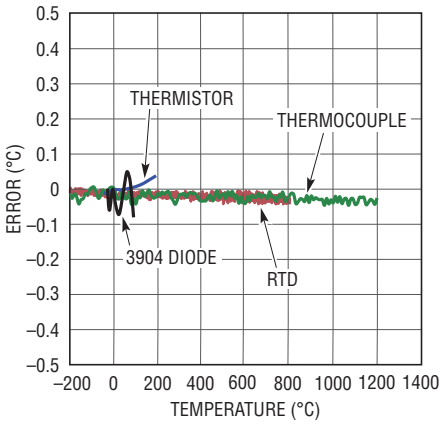


Figure 1. Typical temperature error conformity of the LTC2983 with various sensors

THERMOCOUPLES: WHAT'S IMPORTANT

A thermocouple's generated output voltage is small (< 100mV full-scale) (see Figure 2). As a result, the offset and noise of the ADC making the voltage measurement must be low. Furthermore, it is an absolute voltage reading requiring an accurate/low drift reference voltage. The LTC2983 contains a low noise, continuously offset calibrated 24-bit delta-sigma ADC (offset and noise <1µV) with a 10ppm/°C max reference (see Figure 3).

A thermocouple's output voltage can also go below ground when the tip is exposed to temperatures below the cold junction temperature. This complicates systems by either forcing the addition of a second negative supply or an input level shifting circuit. The LTC2983 incorporates a proprietary front end capable of digitizing signals below ground on a single ground-referenced supply.

In addition to high accuracy measurements, thermocouple circuits need to incorporate noise rejection, input protection, and anti-alias filtering. The LTC2983 input impedance is high, with a maximum input current of less than 1nA. It can accommodate external protection resistors and filtering capacitors without introducing extra errors. It includes an on chip digital filter with 75dB rejection of both 50Hz and 60Hz or 120dB of 50Hz or 60Hz.

Fault detection is an important feature of many thermocouple measurement systems. The most common fault reported is an open circuit (broken or unplugged thermocouple). Historically, current sources or pull-up resistors were applied to the thermocouple input in order to detect this type of fault. The problem with this approach is that these induced

If two perfectly matched excitation current sources of known ratio are applied to the diode, a voltage of known proportionality to absolute temperature (PTAT) is output. The LTC2983 automatically generates the ratioed currents, measures the resultant diode voltage, calculates the temperature using the programmed non-ideality and outputs the results in °C. It can also be used as the cold junction sensor for thermocouples.

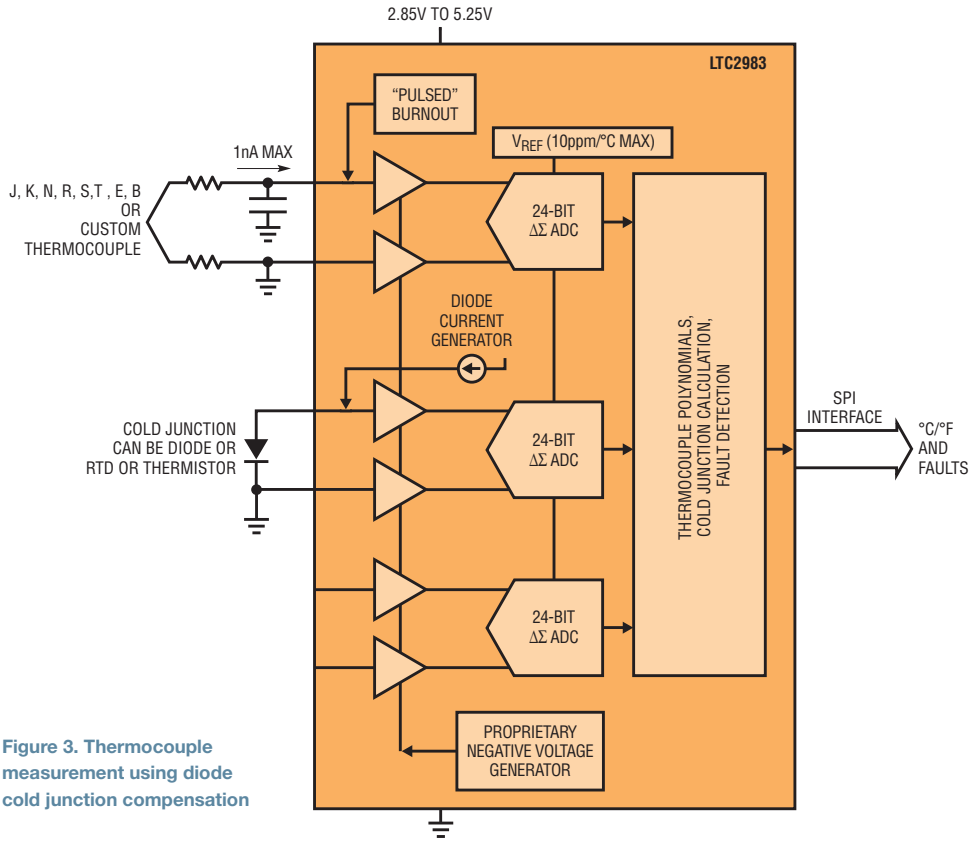


Figure 3. Thermocouple measurement using diode cold junction compensation

signals lead to errors and noise, and interact with input protection circuitry.

The LTC2983 includes a unique open circuit detection circuit that checks for a broken thermocouple just prior to the measurement cycle. In this case, the open circuit excitation current does not interfere with measurement accuracy. The LTC2983 also reports faults related to the cold junction sensor. It can detect, report and recover from electrostatic discharge (ESD) events that may occur when long sensor connections are used in industrial environments. The LTC2983 indicates via fault reporting if the measured temperature is above/below the expected range for the specific thermocouple.

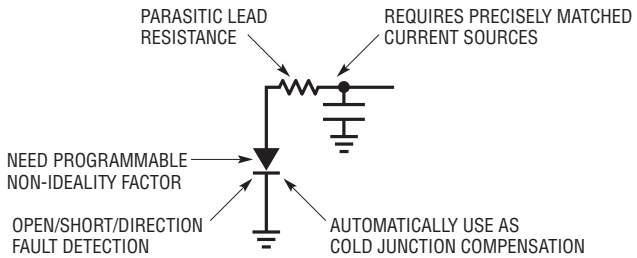


Figure 4. Diode design challenges

DIODES: OVERVIEW

Diodes are inexpensive semiconductor-based devices that can be used as temperature sensors. These devices are typically used as the cold junction sensor for a thermocouple. When an excitation current is applied to a diode, they generate a voltage as a function of temperature and the current that is applied. If two perfectly matched excitation current sources of known ratio are applied to the diode, a voltage of known proportionality to absolute temperature (PTAT) is output.

DIODES: WHAT'S IMPORTANT

In order to generate a PTAT voltage with known proportionality, two highly matched, ratioed current sources are required (see Figure 4). The LTC2983 accurately generates this ratio by relying on delta-sigma oversampling architecture. Diodes and the leads connecting to the ADC contain unknown parasitic diode effects. The LTC2983 contains a 3-current measurement mode that removes parasitic lead resistances. Various diode manufacturers specify different diode non-ideality factors. The LTC2983 allows individual programming of each diode's non-ideality factor. Since absolute voltages are measured, the value and drift of the ADC reference voltage are critical. The LTC2983 includes a factory trimmed 10ppm/°C max reference.

For RTDs, the LTC2983 automatically generates the excitation current, simultaneously measures the sense resistor and RTD voltage, calculates the sensor resistance and reports the result in °C. The LTC2983 can digitize most RTD types (PT-10, PT-50, PT-100, PT-200, PT-500, PT-1000 and NI-120) and has built in coefficients for many standards (American, European, Japanese and ITS-90).

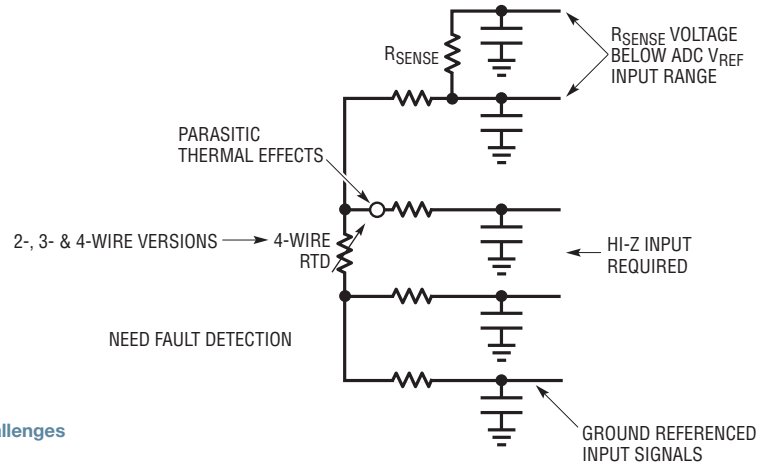


Figure 5. RTD design challenges

The LTC2983 automatically generates the ratioed currents, measures the resultant diode voltages, calculates the temperature using the programmed non-ideality and outputs the results in °C. It can also be used as the cold junction sensor for thermocouples. If the diode is broken, shorted or inserted incorrectly, the LTC2983 detects this fault and reports it in the conversion result output word and the corresponding thermocouple result, if it was used to measure the cold junction temperature.

RTDs: OVERVIEW

RTDs are resistors that change value as a function of temperature, and can measure temperatures over a wide temperature range, from as low as –200°C to 850°C. In order to measure one of these devices, a low drift, precision sense resistor is tied in series with the RTD. An excitation current is applied to the network and a ratiometric measurement is made. The value, in ohms, of the RTD can be determined from this ratio. This resistance is used to determine the temperature of the sensor element using a table lookup.

The LTC2983 automatically generates the excitation current, simultaneously measures the sense resistor and RTD voltage, calculates the sensor resistance and reports the result in °C. The LTC2983 can digitize most RTD types (PT-10, PT-50, PT-100, PT-200, PT-500, PT-1000 and NI-120) and has built in coefficients for many standards (American, European, Japanese and ITS-90).

RTDs: WHAT'S IMPORTANT

A typical PT100 RTD (see Figure 5) resistance varies less than 0.04Ω per tenth of 1°C corresponding to a signal level of 4µV at 100µA current excitation. Low ADC offset and noise are critical for accurate measurements. The measurement is ratiometric relative to the sense resistor; the absolute values of the excitation current and reference voltage are not as important when calculating the temperature.

Historically, the ratiometric measurement between the RTD and sense resistor was performed with a single ADC. The sense resistor's voltage drop was used as the reference input of the ADC measuring the RTD voltage drop. This architecture requires 10k or larger sense resistors, which must be buffered to prevent droop due to the ADC reference input dynamic currents. Since the sense resistor value is critical, these buffers need to have low offset, drift and noise. This architecture makes it difficult to rotate current sources in order to remove parasitic thermocouple effects. Delta-sigma ADC reference inputs are much more susceptible to noise than the inputs, and small values of reference voltage can lead to instability.

These problems are solved by the LTC2983's multiple ADC architecture (see Figure 6). The LTC2983 uses two highly matched, buffered, auto-calibrated ADCs, one for the input and one for the reference. They simultaneously measure both RTD and R_{SENSE}, calculate

The LTC2983 includes coefficients for calculating the temperature of standard 2.252k, 3k, 5k, 10k and 30k thermistors. Since there is a large variety of thermistor types and values, the LTC2983 can be programmed with custom thermistor table data (R vs T) or Steinhart-Hart coefficients.

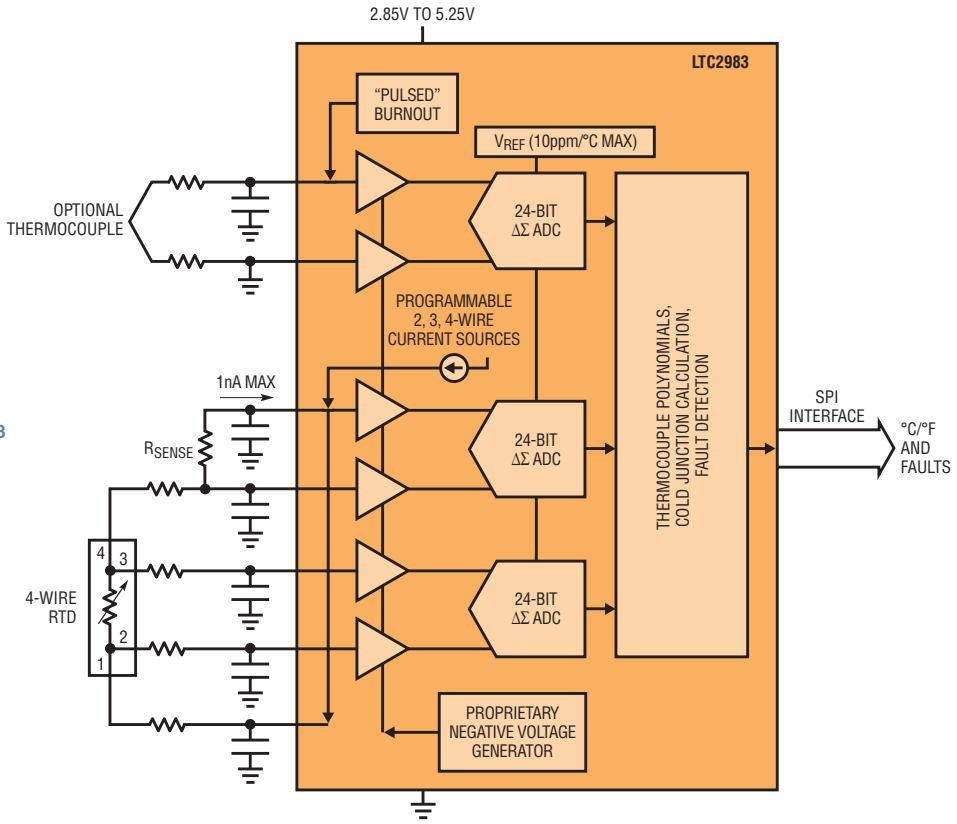


Figure 6. RTD temperature measurement using the LTC2983

the RTD resistance and apply this to a ROM-based lookup table to ultimately output the RTD temperature in °C.

RTDs come in several configurations: 2-wire, 3-wire and 4-wire. The LTC2983 accommodates all three configurations with a configurable single hardware implementation. It can share a single sense resistor among multiple RTDs. Its high impedance input allows external protection circuits between the RTD and ADC inputs without introducing errors. It can also autorotate the current excitation to eliminate external thermal errors (parasitic thermocouples). In cases where parasitic lead resistance of the sense resistor degrades performance, the LTC2983 allows Kelvin sensing of R_{SENSE}.

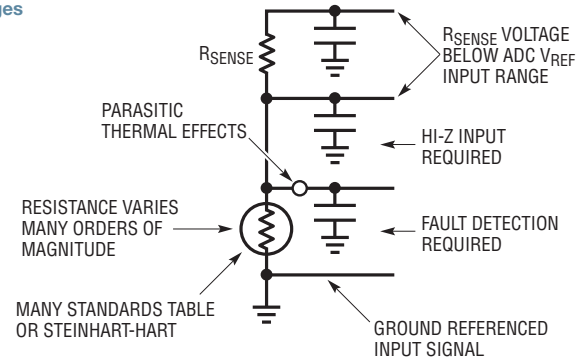
The LTC2983 includes fault detection circuitry to determine if the sense resistor or RTD is broken or shorted. It warns if the measured temperature is above or below the maximum specified for the RTD. When an RTD is used as the cold junction sensor for a thermocouple, three ADCs simultaneously measure the thermocouple, the sense resistor and the RTD. RTD faults are passed to the thermocouple result and the RTD temperature is automatically used to compensate for the cold junction temperature.

THERMISTORS: OVERVIEW

Thermistors are resistors that change value as a function of temperature. Unlike an RTD, a thermistor's resistance varies many orders of magnitude over their temperature range. In order to measure one of these devices, a sense resistor is tied in series with the sensor. An excitation current is applied to the network and a ratiometric measurement is made. The value, in ohms, of the thermistor can be determined from this ratio. This resistance is used to determine

The LTC2983 includes fault detection circuitry that can determine if the sense resistor or thermistor is broken/shorted. It warns if the measured temperature is above or below the maximum specified for the thermistor.

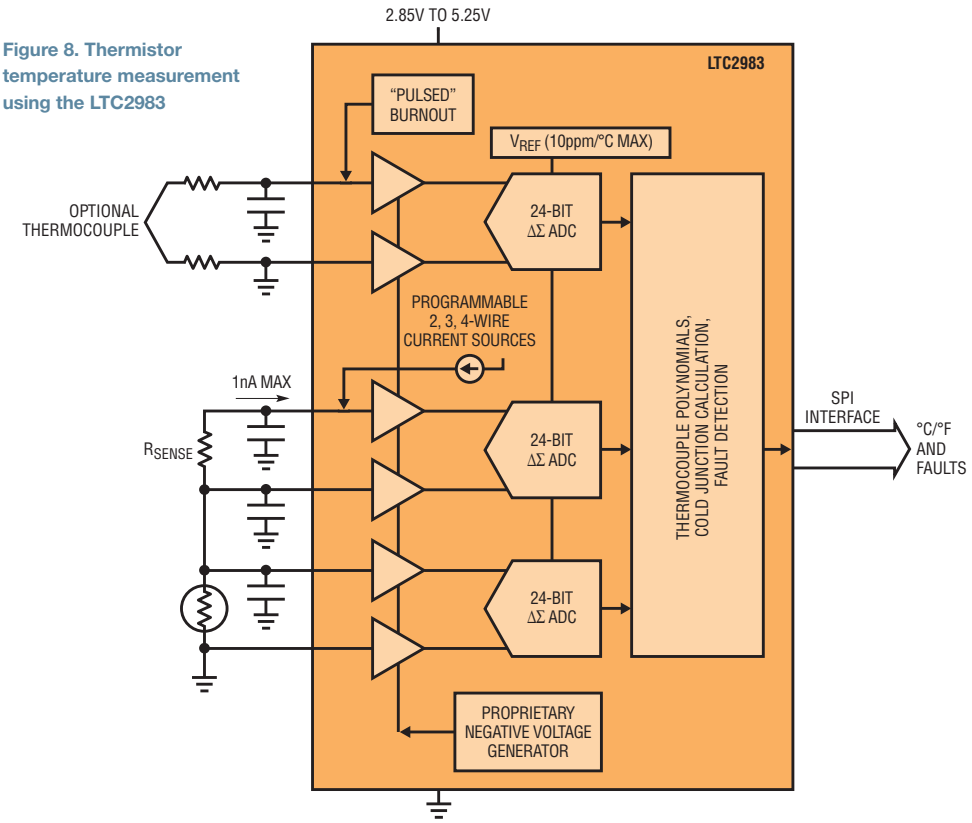
Figure 7. Thermistor design challenges



the temperature of the sensor solving Steinhart-Hart equations or table data.

The LTC2983 automatically generates the excitation current, simultaneously measures the sense resistor and thermistor voltage, calculates the thermistor's resistance and reports the result in °C. Thermistors typically operate from –40°C to 150°C. The LTC2983 includes coefficients for calculating the temperature of standard 2.252k, 3k, 5k, 10k and 30k thermistors. Since there is a large variety of thermistor types and values, the LTC2983 can be programmed with custom thermistor table data (R vs T) or Steinhart-Hart coefficients.

Figure 8. Thermistor temperature measurement using the LTC2983



THERMISTORS: WHAT'S IMPORTANT

A thermistor's resistance (see Figure 7) varies many orders of magnitude over its temperature range. For example, a thermistor measuring 10k at room temperature can go as low as 100Ω at its highest temperature and > 300k at its lowest, while other thermistor standards can go above 1M.

Typically, in order to accommodate large valued resistance, very small excitation current sources are used in conjunction with large sense resistors. This results in very small signal levels at the low end of the thermistor's range. Input and reference buffers are required to isolate the ADC's dynamic input current from these large resistors. But buffers don't work well near ground without separate supplies and offset/noise errors need to be minimized.

These problems are all solved by the LTC2983 (see Figure 8). It combines a proprietary, continuously calibrated buffer capable of digitizing signals at or even below ground with its multiple ADC architecture. Two matched, buffered ADCs simultaneously measure the thermistor and sense resistor and calculate (based on the standard) the thermistor temperature in °C. Large value sense resistors are not required, allowing multiple RTDs and thermistors of different types to share a single sense resistor. The LTC2983 can also

The LTC2983 is a groundbreaking, high performance integrated temperature measurement system that directly digitizes thermocouples, RTDs, thermistors and diodes with laboratory grade precision. It features high accuracy, an easy sensor interface and tremendous flexibility.

auto-range the excitation current depending on the thermistor's output resistance.

The LTC2983 includes fault detection circuitry that can determine if the sense resistor or thermistor is broken/shorted. It warns if the measured temperature is above or below the maximum specified for the thermistor.

The thermistor can be used as the cold junction sensor for a thermocouple. In this case, three ADCs simultaneously measure the thermocouple, the sense resistor and the thermistor. Thermistor faults are passed to the thermocouple result and the thermistor temperature is automatically used to compensate the cold junction temperature.

UNIVERSAL MEASUREMENT SYSTEM

The LTC2983 can be configured as a universal temperature measurement device (see Figure 9). Up to four sets of universal inputs can be applied to a single LTC2983. Each of these sets can directly digitize a 3-wire RTD, 4-Wire RTD, thermistor or thermocouple without changing any onboard hardware. Each sensor can share the same four ADC inputs and protection/filtering circuitry, configured using software. One sense resistor is shared among all four banks of sensors and cold junction compensation is measured by a diode. The LTC2983 input structure allows any sensor on any channel. Any combination of RTDs, sense resistors, thermistors, thermocouples, diodes and cold junction compensation can be applied to any and all the 21 analog inputs on the LTC2983.

CONCLUSION

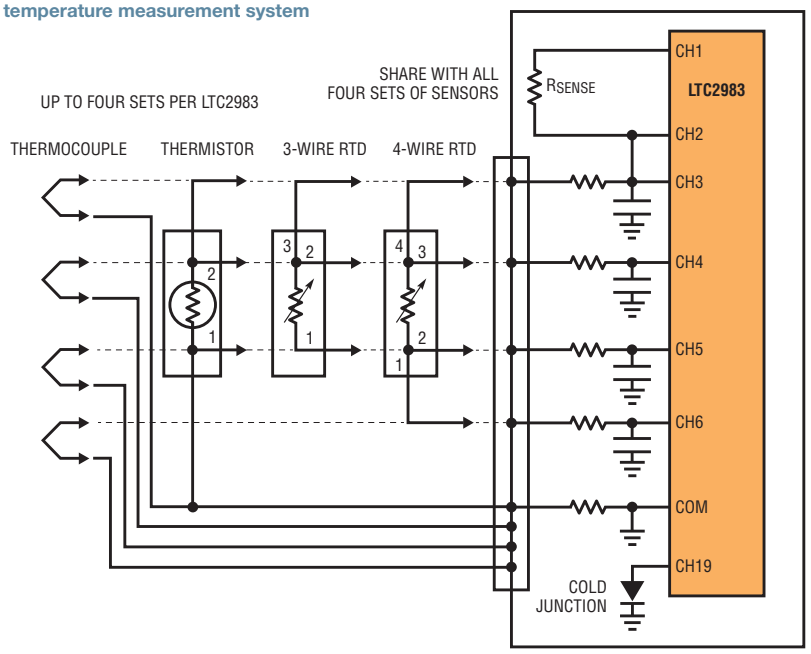
The LTC2983 is a groundbreaking, high performance integrated temperature measurement system that directly digitizes thermocouples, RTDs, thermistors and diodes with laboratory grade precision. It features high accuracy, an easy sensor interface and tremendous flexibility.

Its three 24-bit delta-sigma ADCs use a proprietary front end to solve many problems typically associated with temperature measurements. High input impedance with live-at-zero input range enables direct digitization of all temperature sensors and easy input projection. Twenty flexible analog inputs allow a single hardware design to measure any sensor by simply reprogramming the device through the SPI interface.

The LTC2983 automatically performs cold junction compensation, can use any sensor to measure the cold junction and includes fault reporting. It can directly measure 2-, 3- or 4-wire RTDs, and can easily share sense resistors to save cost and rotate current sources to remove parasitic thermal effects. It includes auto-ranging current sources for increased accuracy and reduced noise associated with thermistor measurements.

In addition to the built-in sensor profiles, the LTC2983 enables custom, user-programmable sensor profiles to account for nonstandard, table-driven RTDs, thermocouples and thermistors. ■

Figure 9. Universal temperature measurement system



SPICE Differentiation

Mike Engelhardt

To download LTspice, go to www.linear.com/ltspice

Analog design engineers lean heavily on simulation to predict circuit performance. The value of a simulator hangs on how well it can predict physical reality, and how quickly it can produce results. Discrepancy between simulated and real performance can send a product into costly iterative debugging cycles.

SPICE is used for analog circuit simulation because it can compute the full large signal behavior of arbitrary circuits. Three numerical methods used in SPICE account for its success in analog circuit simulation. Specifically:

- *Newton iteration* to find the solution of circuits with nonlinear elements
- *Sparse matrix* methods to corral huge matrices into the address space of a practical computer
- *Implicit integration* to integrate the differential equations that arise from circuit reactances

The ability of a SPICE simulator to reliably produce correct results depends on how well these methods are implemented. This article outlines why LTspice is better at yielding correct results than other SPICE implementations.

NEWTON ITERATION

Newton iteration involves expanding each nonlinear circuit device I-V curve as a Taylor series but keeping only the first two terms and then solving the resultant system of simultaneous linear equations. If the solution of the linear system is indeed the very point about which the Taylor series was expanded, then, because the Taylor approximation is exact at that point and accurate near it, the solution of this linear system is in fact the correct solution to the original nonlinear circuit.[1] Success of convergence of Newton iteration results in finding a numerical proof that the correct solution of your circuit was found.

Robustness of Newton iteration depends on (1) having all circuit element I-V curves being continuous in value and slope and (2) all nonlinear elements being bypassed with capacitance so that the previous time step solution is a good starting point for the Newton iteration of the current time point. Conditions (1) and (2) are met by any physical circuit, but SPICE programs usually don't get this right because the semiconductive devices in Berkeley SPICE have discontinuities and these implementation errors have spilled over to pay-for SPICE implementations. These discontinuities do not occur in LTspice. To illustrate an example, Figure 1 shows the I-V curve of a diode in PSpice[2] versus LTspice. The netlist used in each case is

```
* I-V discontinuity in PSpice diode
V1 N001 0 0
D1 N001 0 D
.dc V1 -.3 -.2 2u
.probe
.model D D(Is=10n)
.end
```

The PSpice diode I-V curve is discontinuous in both value and slope. Such discontinuities exist in most of the semiconductive devices in PSpice but none of the semiconductive devices in LTspice.

SPARSE MATRIX METHODS

The Taylor series is multidimensional—one dimension for each unknown voltage node in the circuit. For an analog IC, this can be 100,000 distinct voltage nodes, leading to a conductivity matrix of 100,000 by 100,000, or *eighty billion* bytes for double precision matrix coefficients. Even today's 64-bit processors don't bond out enough address lines to access that much memory. Fortunately, almost every coefficient is zero, so they don't need to be stored. Sparse matrix methods keep track of only the nonzero elements. This allows a huge matrix to be solved in a comparatively tiny address space.

The sparsity of the matrix arises from the physical nature of practical circuits. Most nodes are only connected to a few other nodes. For example, even if you write out the conductively matrix of a circuit that looks like a fishnet grid of resistors, the matrix is almost diagonal because each node is resistively connected only to adjacent nodes. Practical circuits aren't as dense with connections as fishnets are with knots. The sparsity of a large analog circuit is in the parts per million range. This sparsity is what allows the matrix to be solved in a present day computer. Newton iteration of analog circuits is not possible without sparse matrix methods.

LTspice eliminates the overhead in getting the data to the FPU with self-authoring assembly language source written at run time, after matrix memory has been allocated, and the addresses returned from malloc() are known. This late-authored code can resolve concrete matrix element addresses in line with the code so the data can be efficiently loaded, allowing the FPU to operate with the pipeline full.

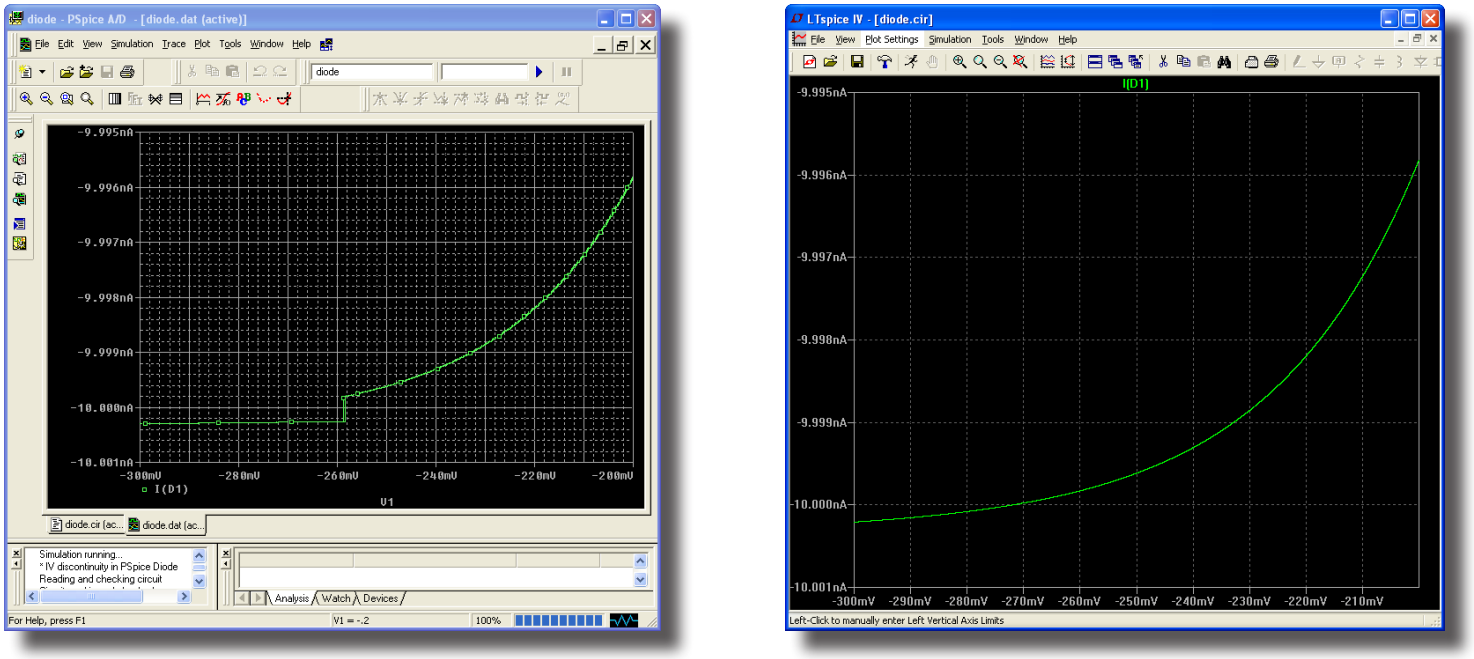


Figure 1. Discontinuity in PSpice (left) diode I-V curve vs continuous diode I-V curve in LTspice (right). Discontinuities negatively impact a simulator's ability to solve nonlinear circuits.

The greatest similarity across SPICE implementations is in these sparse matrix methods. All SPICE programs use LU factorization. Most SPICE implementations use a sparse matrix library derived from the code distributed with the academic Berkeley SPICE code, but some, usually marketed as a fast SPICE, try to improve on it by using an enhanced sparse matrix library such as SuperLU.[3]

A better approach is to simply to get the processor to do the math at the theoretical FLOP limit of the underlying hardware. The issue is that it takes longer to get the numerical data to the FPU than it does to actually perform the FLOP.

The FPU pipeline usually runs empty. Ultimately, this is a consequence of the fact that all operating systems use dynamic memory allocation. At the time the simulator is written and compiled, the memory location storing the matrix data isn't known. At run time the simulator requests memory with function call malloc(), which returns an address at which the simulator is allowed to safely store matrix data. Since it isn't humanly possible to give each matrix element its own name, arrays are used. This means the simulator asks for fewer, but larger, pieces of memory, and the individual coefficients are indexed off the base address returned by malloc(). All that is known at simulator compile time is the address of the address of the base address off which one indexes to reach the matrix element. Resolving this address at run time and fetching the data pointed to by that address into the FPU takes longer than executing the FLOP itself.[4] Ideally, the addresses of the data required for a calculation would be known ahead of calculation time so that data can be efficiently fetched and the FPU doesn't have to wait for it.

LTspice eliminates the overhead in getting the data to the FPU with self-authoring assembly language source written at run time, after matrix memory has been allocated, and the addresses returned from malloc() are known. This late-authored code can resolve concrete matrix element addresses in line with

PSpice's Gear integration method often fails. Gear integration doesn't just dampen numerical ringing, it dampens all ringing, even physical ringing, making it possible for a circuit that malfunctions in real life, due to an oscillation, to simulate as perfectly stable and functional because the instability was damped out of numerical existence.

the code so the data can be efficiently loaded, allowing the FPU to operate with the pipeline full once the code is assembled and linked with LTspice's built-in assembler and linker. LTspice is unique in implementing a self-authoring, self-assembling and self-linking sparse matrix solver. The method performs remarkably better than any other technique.

IMPLICIT INTEGRATION

Analog circuit simulation requires numerical integration of differential equations to track the behavior of the capacitances and inductances. This is where one sees some of the largest differences between one SPICE implementation and another: the method(s) available for integrating the differential equations.

Numerical integration involves error. Analog circuit simulation entails integrating the behavior of many time constants. The nature of integrating differential equations that have solutions that look like exp(-const*time) is that the errors will in fact add up to infinity unless a numerical method called implicit integration is used.[5] Without implicit integration, transient analysis would not be possible in SPICE.

SPICE uses second order integration. Most SPICE implementations follow Berkeley SPICE and provide two forms of second order implicit integration: Gear and trapezoidal (trap).[6] Trap integration is both faster and more accurate than Gear. But trap integration can give rise to a numerical artifact where the integrated discrete time step solution oscillates time step to time step about the true continuous-time

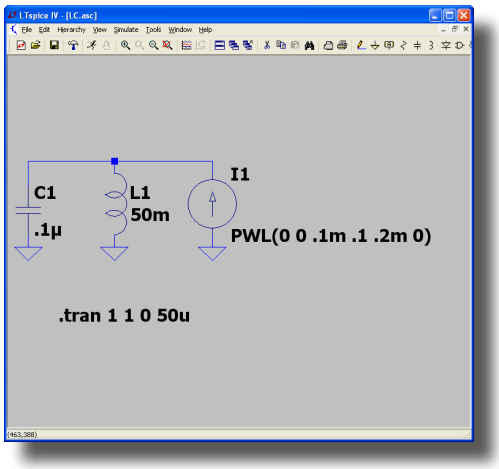


Figure 2. Simple circuit with solution known by inspection

behavior. This can cause the user to be suspicious of the correctness of the simulator even though each trapezoid contains the correct integrated area.

Trap ringing has been feared to be so unacceptable to analog circuit designers [7] that trap integration has been eliminated from one commercial SPICE implementation, PSpice, leaving the slower and less accurate Gear integration as the only available option.

But Gear integration doesn't just dampen numerical ringing, it dampens all ringing, even physical ringing, making it possible for a circuit that malfunctions in real life, due to an oscillation, to simulate as perfectly stable and functional because the instability was damped out of numerical existence. This has led to disastrous situations where an IC design is simulated in PSpice, laid out, and fabricated only to find that the circuit doesn't function due to an instability that PSpice's Gear integration missed. A mask revision cycle—at considerable expense in time and treasure—is required to remove the instability to try to achieve initial functionality.

In principle, Gear integration error could be reduced by having the IC designer stipulate a small maximum time step. But this is not a viable solution because (1) small time steps slow simulation speed to a crawl and (2) there's no way to ensure that the time step is small enough anyway.

PSpice's documentation states that it uses a modified Gear method and does indeed seem better at picking a small enough time step to reduce the error than the Gear integration implementation in Berkeley SPICE.

But PSpice's method often fails. It is easy to compose a trivial circuit and see the PSpice numerically integrated result deviate dramatically from the true solution than can be found by inspection. Consider Figure 2, which shows a parallel tank circuit with a parallel piecewise linear current source. The current source asserts a spike of current over the first 0.2ms and is zero thereafter. The solution should be that the tank circuit resonance is excited by the spike of current and thereafter ring at constant amplitude. The netlist of the circuit is given by

```
* Gear (PSpice) integration error
L1 N001 0 50m
I1 0 N001 PWL(0 0 .1m .1 .2m 0)
C1 N001 0 .1u
.tran 1 1 0 50u
.probe
.end
```

Figure 3 shows that PSpice's modified Gear integration artificially dampens the ringing, whereas LTspice immediately yields

LTspice uses an integration method, modified trap, that has the speed and accuracy of trap but without the ringing artifact. Modified trap is a method I invented some years ago and was widely available first in LTspice. To the best of my knowledge, it is the best means to integrate the differential equations of an analog circuit and is not duplicated in any other SPICE program. It is the only method I recommend for circuit design.

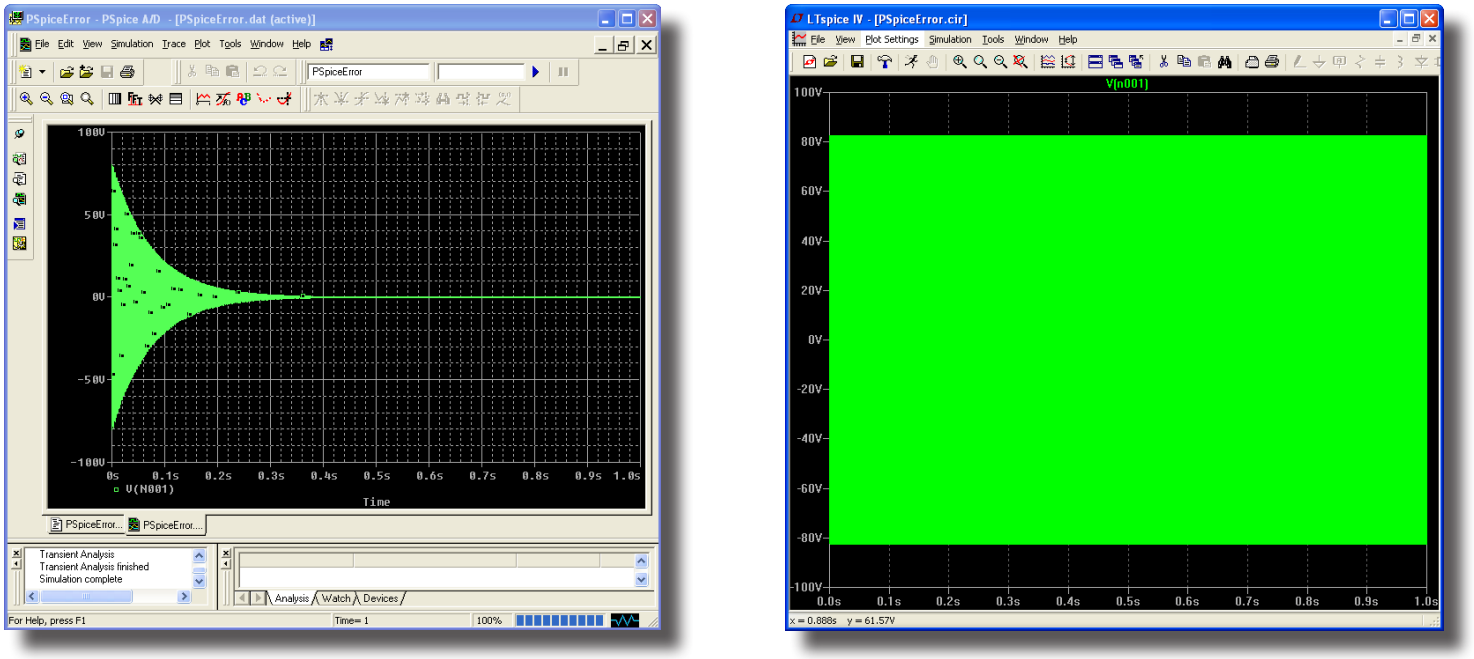


Figure 3. PSpice (left), utilizing modified Gear numerical integration, incorrectly artificially dampens ringing in the circuit of Figure 2. LTspice (right) produces the correct result.

the correct solution. The error in PSpice can be reduced by stipulating a smaller maximum time step (fourth number in the .tran statement). This should be a simple circuit for PSpice's modified Gear to figure out. But a circuit with many different time constants is basically impossible for PSpice to solve reliably without the engineer manually inspecting how the "solution" converges as one stipulates ever smaller maximum time steps.

Figure 3 shows PSpice Gear integration clearly doesn't correctly integrate the two reactances of a trivial circuit with only one node. The nature of the error of Gear integration is to make circuits look more stable in simulation than they actually are in real life. To put the consequences of this error in the perspective of a practical example, Figure 4 shows an audio power amplifier that isn't stable because compensation capacitor C2 is too small.

PSpice incorrectly simulates this circuit as stable, whereas LTspice gives the correct result. The netlist used in each case is

```
* Unstable Power Amplifier
Q5 N001 N006 N007 0 Q3904
Q7 N001 N007 OUT 0 Q2219A
Q8 OUT N013 N014 0 Q2219A
Q6 N013 N012 OUT 0 Q3906
V1 N001 0 10
V2 N014 0 -10
R11 N012 N014 5K
R14 OUT 0 8
R9 N006 N008 2K
R10 N008 N012 1K
Q4 N006 N008 N012 0 Q3904
Q1 N005 N009 N011 0 Q3904
Q2 N002 N010 N011 0 Q3904
R3 N011 N014 1K
Q3 N006 N004 N003 0 Q3906
R6 N010 0 20K
R7 OUT N010 200K
V3 IN 0 pulse(0 .1 0
+ 5u 5u 50u 100u)
R8 N001 N003 100
R4 N004 N005 10K
C2 N006 N004 10p
R13 N013 N014 1K
R12 N007 OUT 1K
C3 N006 N012 .001u
Q9 N005 N002 N001 0 Q3906
Q10 N002 N002 N001 0 Q3906
R2 IN N009 9.09K
.tran 100u 100u
.model Q3904 NPN(Is=1E-14 Vaf=100
+ Bf=300 Ikf=0.4 Xtb=1.5
+ Br=4 Cjc=4p Cje=8p Rb=20 Rc=0.1
+ Re=0.1 Tr=250n Tf=.35n
+ Itf=1 Vtf=2 Xtf=3)
.model Q3906 PNP(Is=1E-14 Vaf=100
+ Bf=200 Ikf=0.4 Xtb=1.5
+ Br=4 Cjc=4.5p Cje=10p Rb=20
+ Rc=0.1 Re=0.1 Tr=250n
+ Tf=.35n Itf=1 Vtf=2 Xtf=3)
.model Q2219A NPN(Is=14.34f
+ Xti=3 Eg=1.11 Vaf=74.03
+ Bf=255.9 Ne=1.307 Ise=14.34f
+ Ikf=.2847 Xtb=1.5
+ Br=6.092 Nc=2 Isc=0 Ikr=0
+ Rc=1 Cjc=7.306p Mjc=.3416
+ Vjc=.75 Fc=.5 Cje=22.01p
+ Mje=.377 Vje=.75 Tr=46.91n
+ Tf=411.1p Itf=.6 Vtf=1.7
+ Xtf=3 Rb=10)
.probe
.end
```

Figure 5 compares PSpice's erroneously stable result (left) with the correct, oscillating result from LTspice (right). The simulation is a large-signal transient analysis of step response. If a small enough time step is stipulated in the PSpice simulation, you can force it to approach the correct solution, suggesting that PSpice is interpreting the device equations of the transistors correctly, PSpice just isn't accurately integrating the differential equations.

What is needed is a method with the speed and accuracy of trap but without the ringing artifact. To this quest, whereas PSpice eliminated trap ringing by using Gear integration but tries to pick a good time step, another approach is to use a de-tuned version of trap integration so that it will damp trap ringing but only introduce a hopefully acceptably small error in the true circuit behavior. It is actually possible, but not recommended, to de-tune LTspice's trap integration with the undocumented option called trapdamp, by adding the SPICE directive

```
.options trapdamp=.01
```

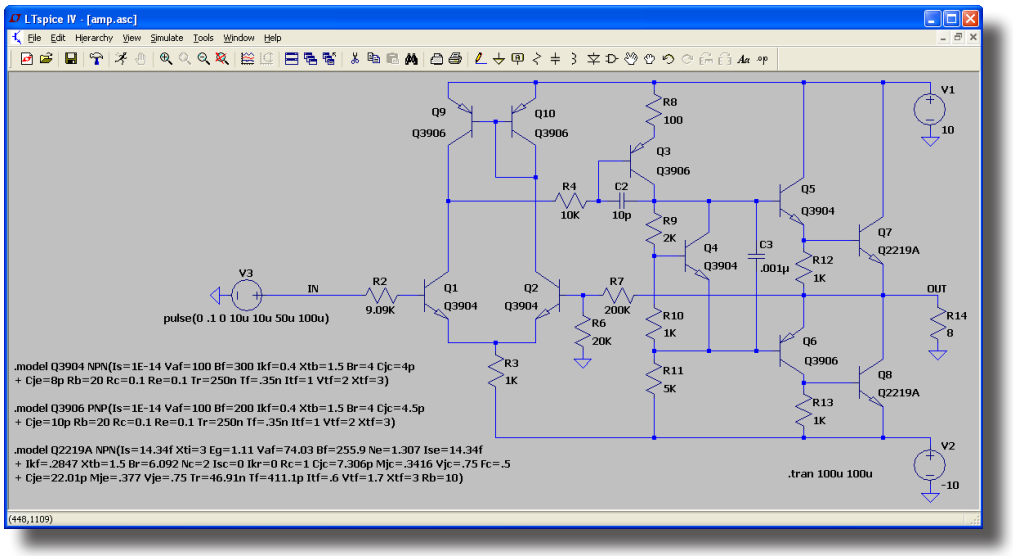


Figure 4. Unstable power amplifier

to your schematic. You might be able to find a value of trapdamp that duplicates the integration behavior of HSPICE[8]. Nevertheless, I do not recommend using this option because it dampens real circuit behavior and it isn't necessary in LTspice, which uses a better method of eliminating trap ringing.

LTspice uses an integration method, modified trap, that has the speed and accuracy of trap but without the ringing artifact. Modified trap is a method I invented some years ago and was widely available first in LTspice. To the best of my knowledge, it is the best means to integrate the differential equations of an analog circuit and is not duplicated in any other SPICE program. It is the only method I recommend for circuit design. LTspice does also support the use of the other known methods,

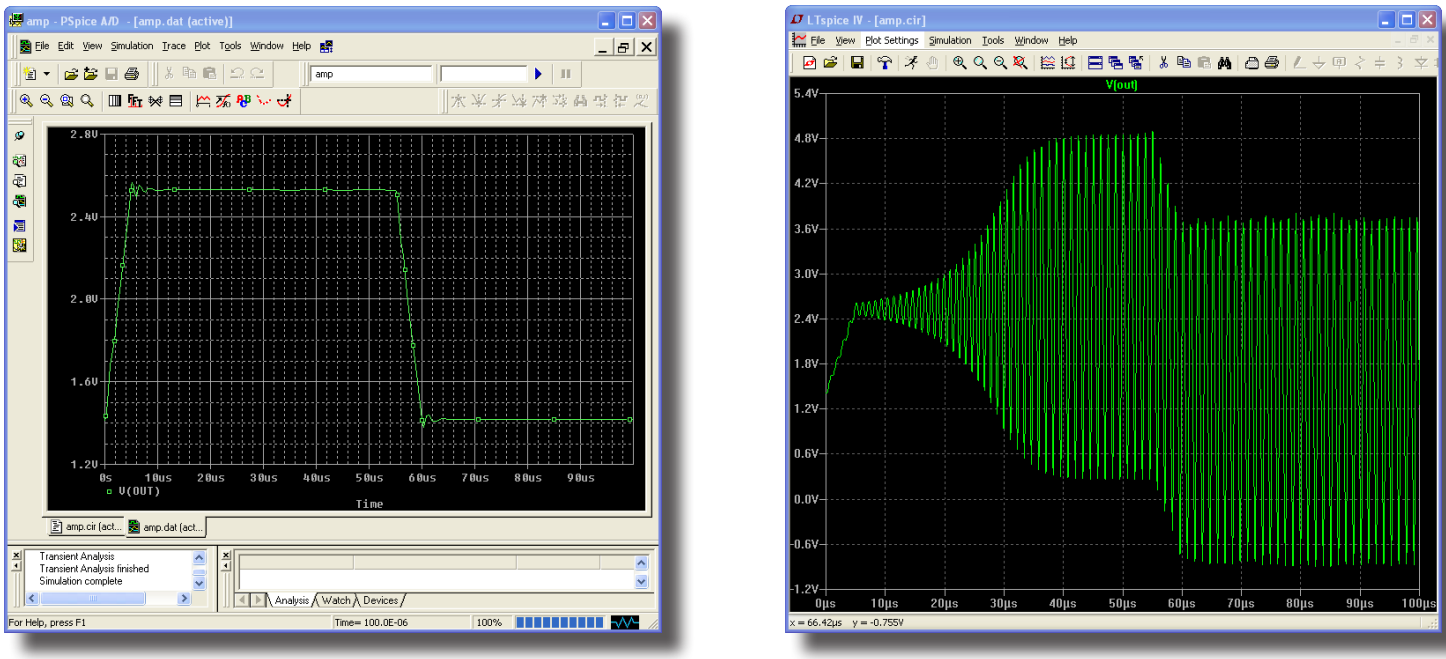


Figure 5. Simulated output from an unstable power amplifier in the face of a large signal transient. PSpice (left) incorrectly indicates the circuit as stable, while LTspice (right) correctly reveals the instability.

trap and Gear, but simply so that a user can duplicate the erroneous results from other SPICE simulators to verify that the models are interpreted the same and only the integration method is different.

Modified trap is used by LTspice to produce Figure 3. Note that there is no change in ringing amplitude even after it rings for thousands of cycles. This demonstrates that LTspice modified trap does not introduce artificial numerical damping. Modified trap is also used by LTspice to produce Figure 5, where LTspice correctly exposes the amplifier's instablity.

To demonstrate the ability of LTspice modified trap to eliminate trap ringing, we need a circuit that is prone to trap ringing. Trap ringing is initiated when discrete time step second order integration has trouble representing the exact continuous-time circuit behavior. It can be reduced or eliminated with judicious use of time step and integration order control.

Since LTspice has been the most popular SPICE program for the last ten years,[9] it has seen a lot of circuits and there is a lot of knowledge libraried into the solver to avoid trap ringing, so one has to work a little to find a counter example. Figure 6 shows a circuit that causes trap ringing due to the highly nonlinear capacitance of the gates of an unusually dimensioned MOSFET inverter. Trap ringing is visible in the gate current drive, I(V1).

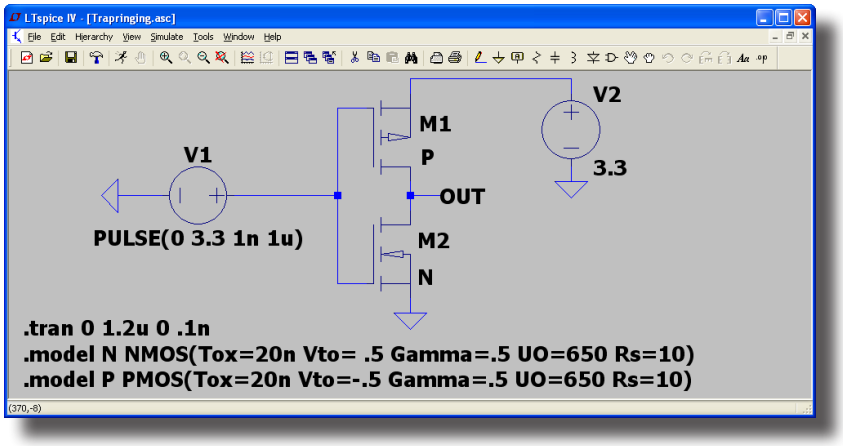


Figure 6. Circuit prone to trap ringing

Figure 7 compares trap integration to LTspice modified trap. The top plot shows a zoomed in region of the bottom plot to clearly show the ringing. If you would like to reproduce this result in LTspice, go to the SPICE pane of the Control Panel and select trapezoidal integration instead of the default, modified trap.

The netlist for this simulation is:

```
* Trap Ringing Example
V2 N001 0 3.3
V1 N002 0 PULSE(0 3.3 1n 1u)
M1 OUT N002 N001 N001 P
M2 OUT N002 0 0 N
.tran 0 1.2u 0 .1n
.model N NMOS(Tox=20n Vto=.5
+ Gamma=.5 UO=650 Rs=10)
.model P PMOS(Tox=20n
+ Vto=-.5 Gamma=.5 UO=650
+ Rs=10)
.probe
.end
```

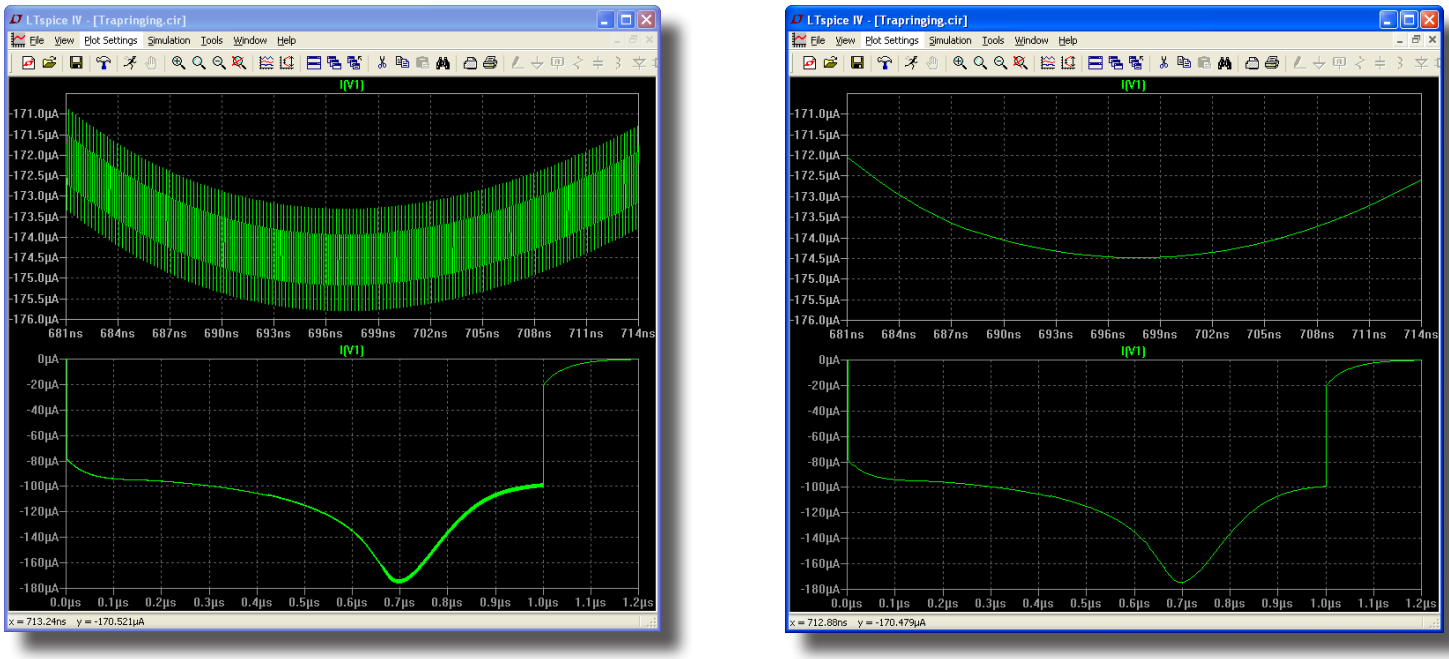


Figure 7. Trap vs LTspice modified trap integration applied to the circuit in Figure 6. Conventional trap integration (left) exhibits trap ringing while the ringing is eliminated with LTspice modified trap (right).

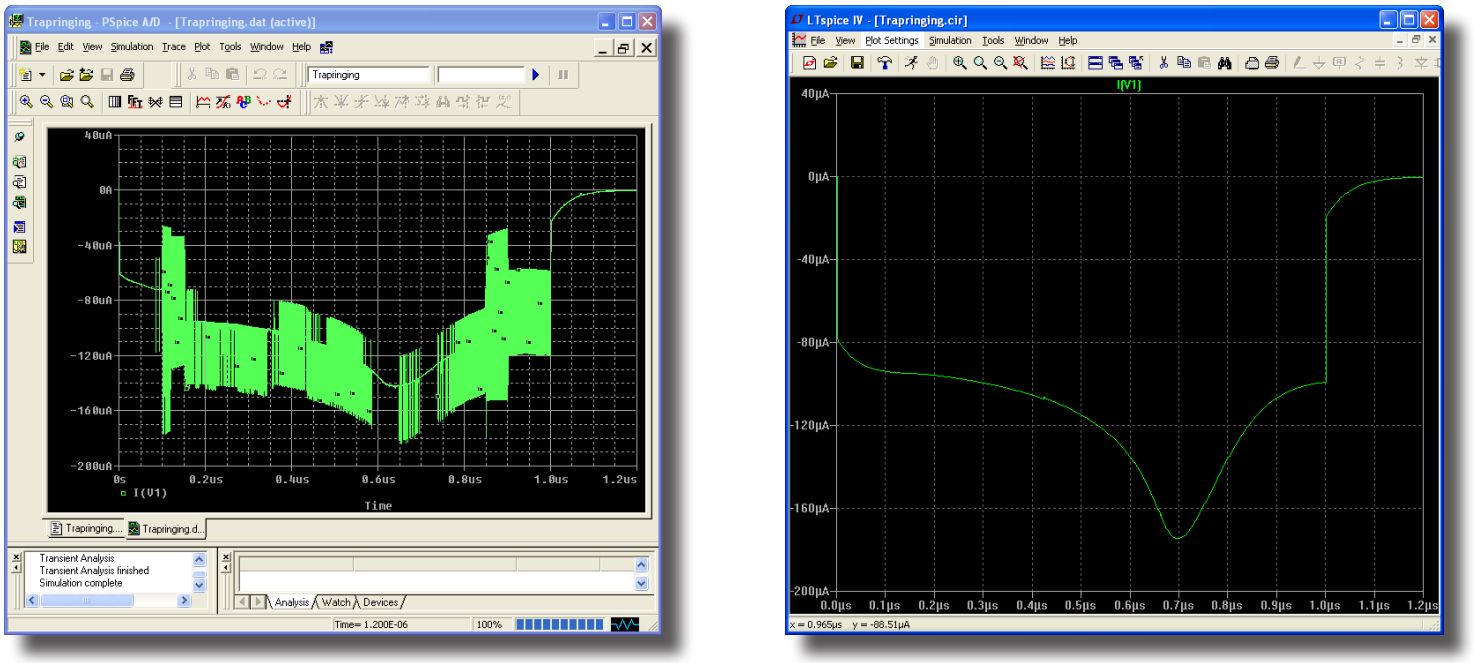


Figure 8. The trap ringing example circuit of Figure 6 run in PSpice (left) does not exhibit trap ringing, but produces other artifacts most likely due to an error in the implementation of the Yang-Chatterjee charge model. LTspice (right) produces the correct result.

Note that most SPICE programs won't run this deck as intended because most SPICE programs use the Meyer capacitance model for this type of MOSFET. Because the Meyer capacitance model doesn't conserve charge and is inaccurate for short channels, it fell into obsolescence in the 1990s.

Both LTspice and PSpice have replaced the Meyer capacitance model with the Yang-Chatterjee charge model. Since both simulators use the same updated charge storage equations, they should give the same results. But when we compare the PSpice simulation to LTspice, as shown in Figure 8, PSpice shows remarkably erroneous results. The oscillations visible in the PSpice simulation, though, are not trap ringing because the oscillation isn't from time step to time step and PSpice doesn't use trap. This artifact is almost certainly due to an error in differentiating the Yang-Chatterjee charge equations to capacitances in the PSpice Yang-Chatterjee charge model implementation.

SUMMARY

LTspice was not the first SPICE implementation, nor is it the only free SPICE, but it is the best and most widely used SPICE implementation.

Newton iteration, sparse matrix methods, and implicit integration are the core numerical methods of SPICE. The simulator's robustness, speed and integrity hinge on how well these methods are implemented.

In the end, a SPICE simulator needs to earn designers' confidence that it can correctly solve for circuit behavior. This is impossible if the solver doesn't perform the core numerical methods correctly. LTspice performs these methods correctly and better than any other SPICE implementation. ■

Notes

[1] Otherwise the solution of the linear system is used as an iteration step: The original nonlinear circuit is re-expanded as a new Taylor series about this solution, again keeping only the first two terms, and then solving the resultant system of simultaneous linear equations. The process repeats until the proof that the correct solution has been found is successful.

[2] PSpice is a Cadence trademark. Version 9.2 was used for the screen shots.

[3] The sparser the matrix, the more closely it can be written as a diagonal, i.e. solved, matrix. Since analog circuit matrices are so sparse, improving LU factorization with SuperLU does not give as much speed advantage as one might hope.

[4] Eliminating the unknowns of a matrix involves mostly addition, subtraction and multiplication. These instructions cost only three latent clock cycles. (There are also some divisions which cost much more than three clocks, but there's only one division per unknown to be eliminated.) Fetching data that is only known by the address of the address of the base address off which one indexes takes much longer than three clock cycles.

[5] Literature on this points out the numerical solution is not singular if a small enough time step is guaranteed, but in practice, an approach with explicit integration and limited time step size doesn't work unless you can numerically integrate with infinite precision. The error doesn't add up to infinity because of round off error but because of approximating the derivative with sampled finite differences. There are no successful general analog circuit simulators that use explicit integration.

[6] SPICE occasionally drops to first order integration, e.g., if an event with a known discontinuous first order time derivative occurs, such as at the transition between two straight line segments of a piecewise linear or pulse function of an independent voltage or current source, most SPICE implementations drop to first order integration for that circuit's reactances at the transition. The first order version of Gear and trap are both backward Euler.

[7] Some users are predisposed to be suspicious of SPICE because of popular literature denigrating the value of SPICE simulation.

[8] HSPICE is a Synopsis trademark.

[9] LTspice is downloaded four times per minute and is the topic of the largest users' group of any simulator. Using distribution and use figures of other SPICE implementations based on private communication with representatives from the respective companies that sell those other SPICE programs, LTspice is distributed and used three orders of magnitude more than any other SPICE program.

1.4GHz Low Jitter PLL with Clock Distribution Solves Difficult Clocking Problems: Multi-Clock Synchronization and Data Converter Clocking

Chris Pearson

Two of the more difficult challenges facing clock system designers are synchronizing multiple system clocks and creating low jitter data converter clocks. The LTC6950 overcomes these challenges by featuring Linear Technology's easy-to-use EZSync™ technology and providing five clock outputs with less than 100fs RMS additive jitter.

Other multi-clock synchronization solutions involve aligning the edges of two or more high speed input signals within an extremely precise time window, sometimes within a couple nanoseconds. Such devices, hinting at the unreliability of this synchronization method, often include a SYNCRESULT pin to indicate whether the synchronization passed or failed, requiring a retry. The elegance of EZSync is it eliminates the need for precision alignment of any high speed input signals, while assuring consistent edge alignment of all outputs on one or multiple EZSync clock devices. With EZSync, synchronizing multiple devices, multiple boards and even multiple system level clock edges is as easy as pressing a button.

The LTC6950 produces five low jitter, high slew rate differential clocks. These clock characteristics allow designers to clock multiple high speed data converters directly, without the typical additional expense of onboard clock filtering and clock shaping components. The LTC6950 simplifies overall system design and cost compared to traditional data converter clock architectures.

The first part of this article summarizes the LTC6950's features and how it works. The second part covers the LTC6950's EZSync functionality. The third part describes the benefits of clocking ADCs and DACs directly with the LTC6950. Finally, a complete LTC6950 design example shows exactly how easy it is to design a typical LTC6950 application using Linear's ClockWizard™ tool.

LTC6950 OVERVIEW

The block diagram in Figure 1 shows how the LTC6950 is divided into three main circuit blocks: the phase-locked loop (PLL) section, the clock distribution section and the digital control section.

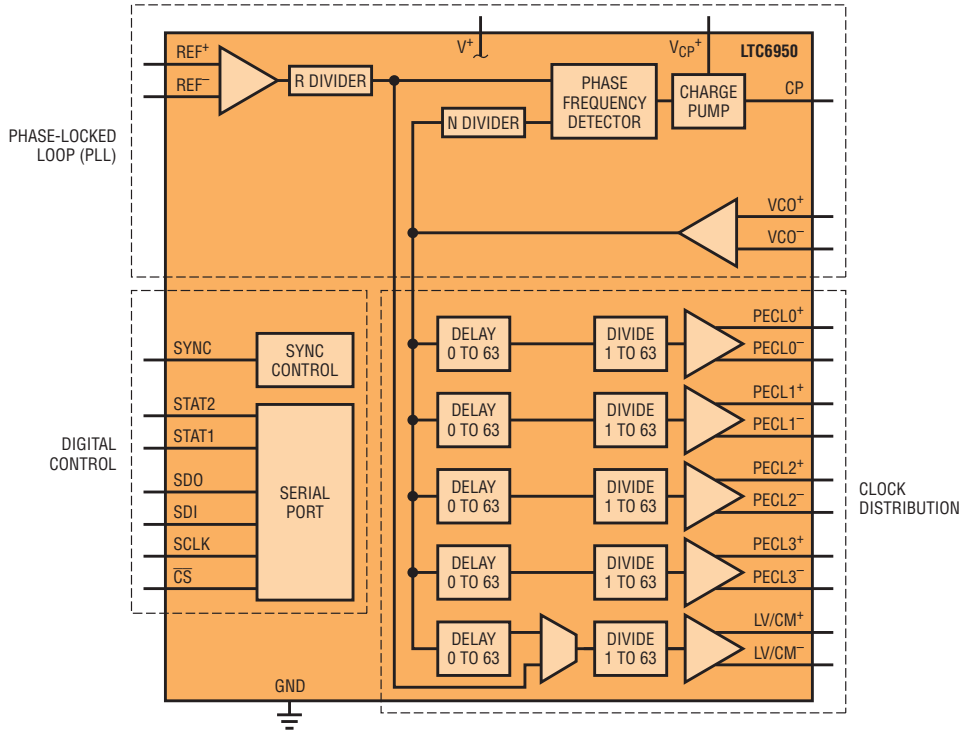
The PLL section works in conjunction with the external reference and external VCO to generate a desired VCO frequency (f_{VCO}) as follows:

$$f_{VCO} = f_{REF} \bullet N/R \quad (1)$$

where f_{REF} is the reference input frequency, R is the reference input divide value and N is the VCO feedback divide value. f_{VCO} is fed into the clock distribution section.

The clock distribution section receives a signal at f_{VCO} and distributes this signal

Figure 1. LTC6950 block diagram



The LTC6950 is the first device to offer Linear Technology's EZSync technology, which simplifies aligning multiple clocks across multiple parts, boards and systems. LTC6950 performance levels enable direct clocking of high performance data converters, simplifying system design and reducing system cost.

to five separate channels. Each of the five channels has the independent ability to delay the first synchronized clock edge by 0 to 63 VCO clock cycles and to divide f_{VCO} by any integer from 1 to 63.

The output signals from the dividers are sent to a buffer that determines the output signal type. Four channels produce an extremely low noise differential LVPECL clock signal capable of output frequencies up to 1.4GHz. The fifth channel creates a configurable differential LVDS output or a pair of CMOS outputs. The LVDS output can produce clock frequencies up to 800MHz, while the CMOS output is limited to 250MHz.

The third and final section is the digital control section. The box labeled SYNC CONTROL in Figure 1 is the EZSync control circuitry—functionality described in detail below. The digital control section includes a standard 4-wire serial interface and two pins to monitor the status of certain register bits.

Figure 2. EZSync STANDALONE mode

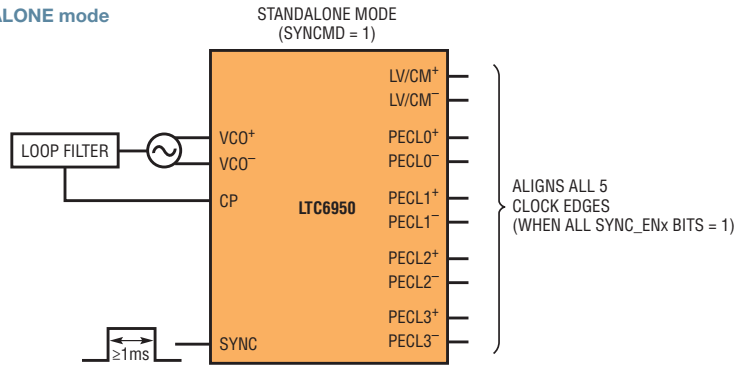
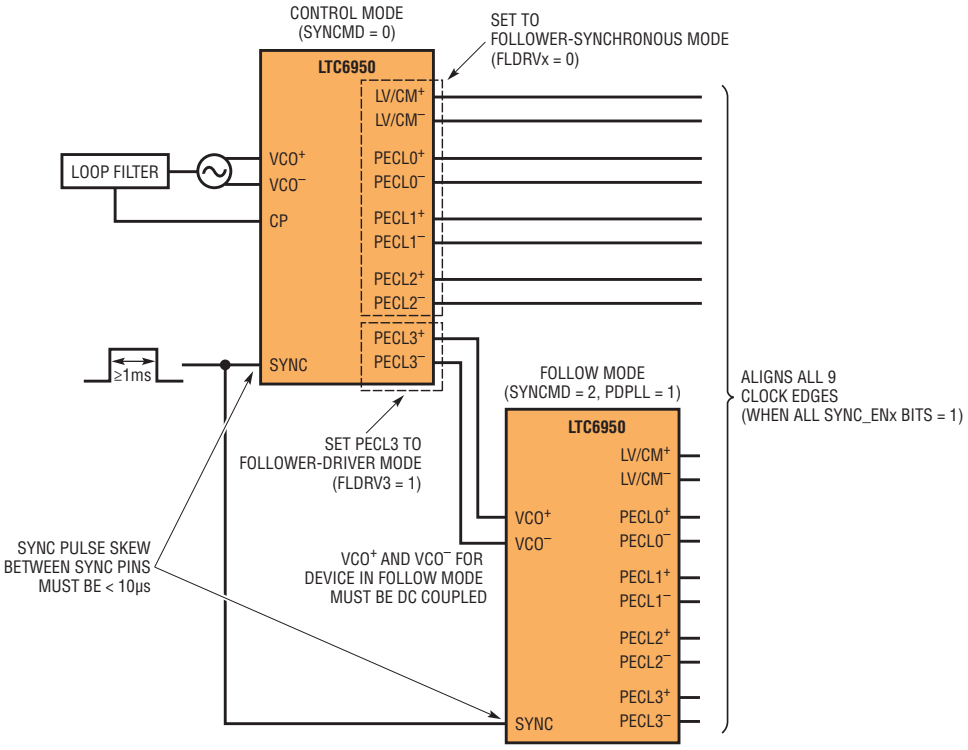


Figure 3. EZSync FOLLOW mode and CONTROL mode using follower-driver and follower-synchronous outputs



EZSync GUARANTEES MULTI-CLOCK SYNCHRONIZATION

As mentioned, synchronizing multiple high speed clocking devices is traditionally difficult due to tight timing constraints and unreliable architectures. In contrast, EZSync guarantees clock synchronization and has relaxed the timing constraints. EZSync functionality is best described visually, as shown in Figures 2, 3 and 4. EZSync has three modes: STANDALONE (Figure 2), CONTROL (Figures 3 and 4), and FOLLOW (Figures 3 and 4).

STANDALONE mode synchronizes the five LTC6950 clock outputs after a 1ms high pulse is applied to the LTC6950 SYNC pin, as shown in Figure 2. Once the SYNC pin goes high, all Sync Enabled clock outputs are held at a logic low once they transition to that state. After the SYNC pin is returned low, all Sync Enabled clock outputs

Linear Technology's ClockWizard tool includes a Scope Plot simulation tool that allows the user to quickly predict the output delay response in the STANDALONE, FOLLOW or CONTROL modes.

resume clocking synchronously. The designer can also chose to disable synchronization on a per output basis by setting the output's SYNC_ENx register bit to a logic low. These outputs will not be disturbed during a synchronization operation.

CONTROL and FOLLOW modes are used in tandem when a LTC6950 clock output is connected to the VCO input of another EZSync device, as illustrated in Figures 3 and 4. Figures 3 and 4 introduce some new terminology: CONTROLLER, FOLLOWER, follower-driver and follower-synchronous, defined below:

- **CONTROLLER:** EZSync device set to CONTROL mode. A device in CONTROL mode controls the timing for all other EZSync devices.
- **FOLLOWER:** EZSync device set to FOLLOW mode. The clock input of a FOLLOWER has a DC coupled connection from a clock output of the CONTROLLER.
- **Follower-Driver:** CONTROLLER's clock output that is connected to a FOLLOWER's clock input. DC coupling is required between the CONTROLLER output and FOLLOWER input.
- **Follower-Synchronous:** CONTROLLER's clock output that is synchronized to its FOLLOWER devices' clock outputs.

In Figure 3, the EZSync CONTROLLER and FOLLOWER architecture synchronizes the four follower-synchronous outputs of the CONTROLLER and the five FOLLOWER outputs after applying a 1ms high pulse to both LTC6950 SYNC pins.

In Figure 4, the EZSync CONTROLLER and FOLLOWER architecture synchronizes 20 FOLLOWER outputs and one follower-synchronous output after applying a 1ms high pulse to all five LTC6950 SYNC pins.

Compared to the STANDALONE architecture, the CONTROLLER and FOLLOWER architecture has an additional modest timing requirement that the max skew between all SYNC signals is < 10µs. The outputs are held in a logic low state during the time the SYNC pin is set to a logic high value and for a few additional VCO cycles after the SYNC pin is returned to a logic low. The user can choose to disable synchronization on any output by setting the appropriate SYNC_ENx register bit to a logic low. These outputs will not be disturbed during a synchronization operation.

MAKING EZSync EASIER

While applying a 1ms high pulse to the LTC6950's SYNC pin is easy, it does require some familiarity with the EZSync specification to predict how the outputs will

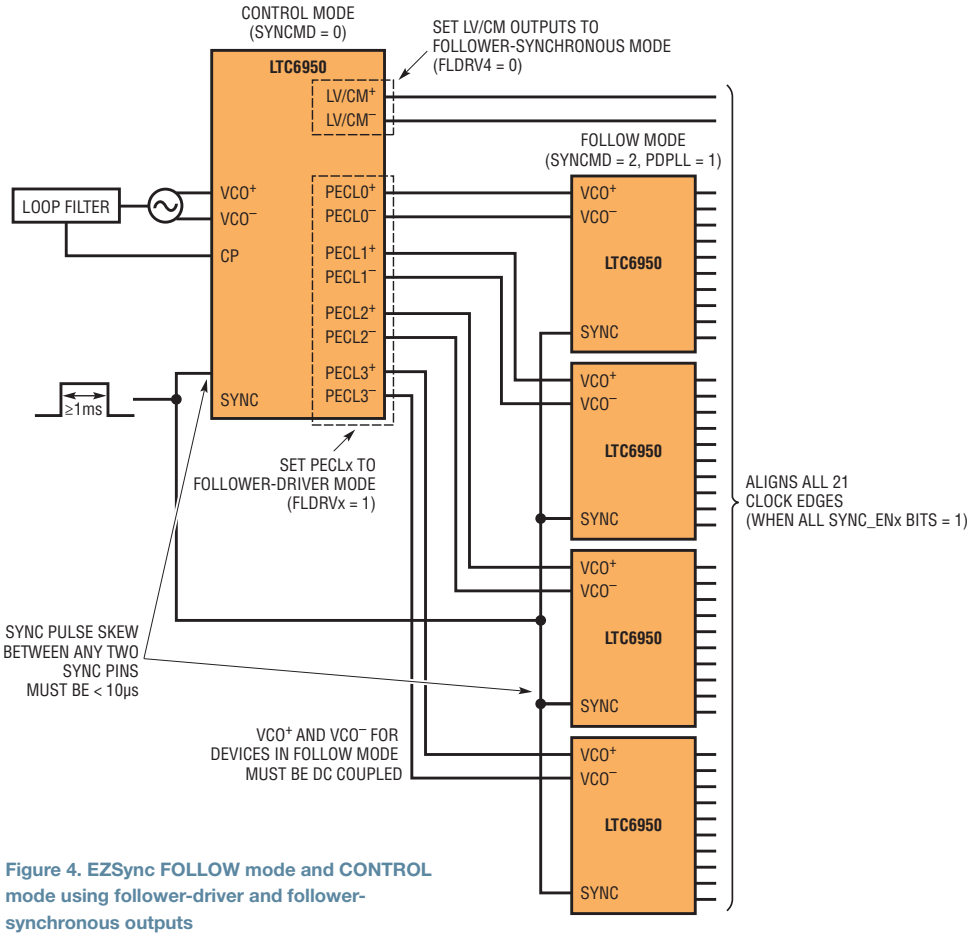


Figure 4. EZSync FOLLOW mode and CONTROL mode using follower-driver and follower-synchronous outputs

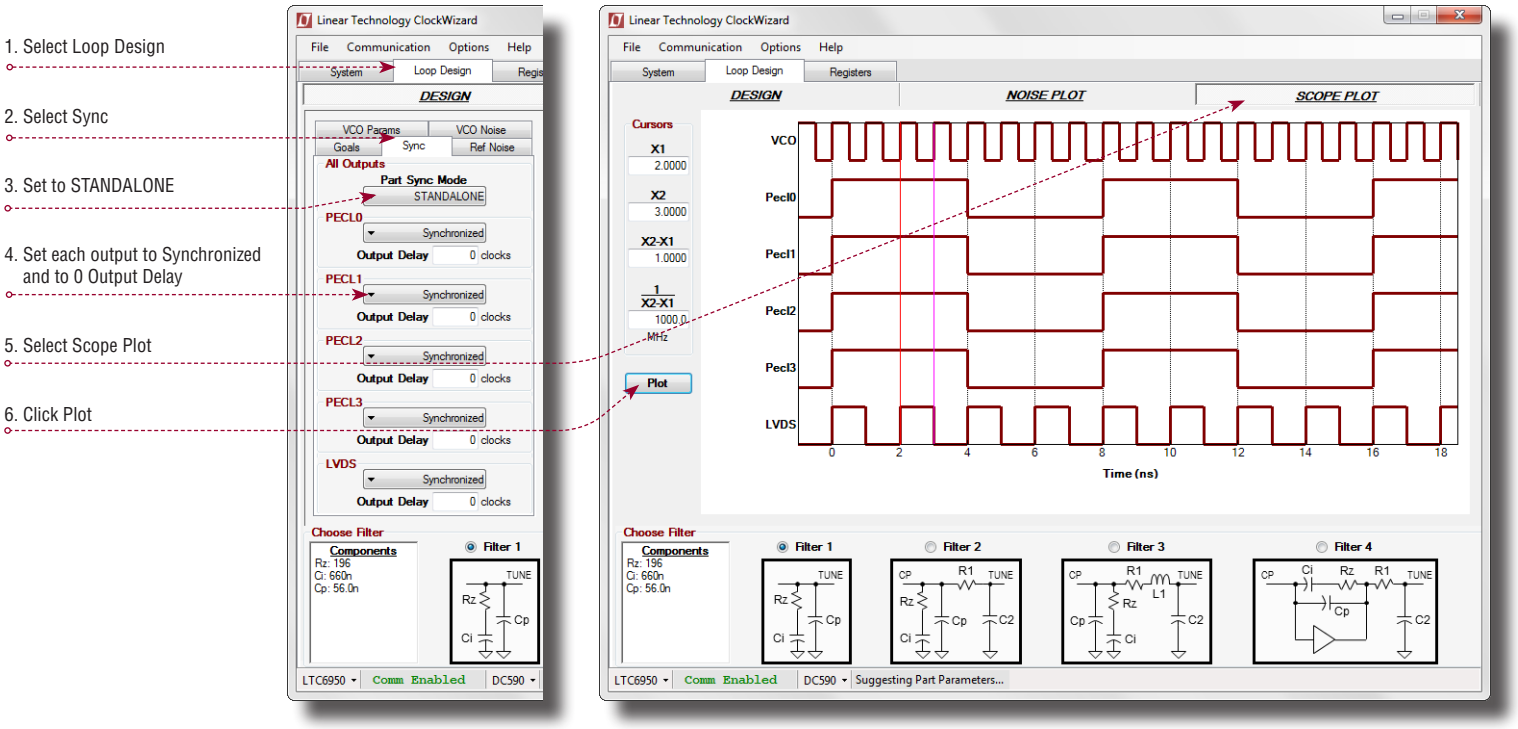


Figure 5. Simulating the LTC6950's output frequencies and output delays in STANDALONE mode using ClockWizard

respond after the LTC6950 SYNC pins are returned to a logic low state. Linear Technology's ClockWizard tool includes a Scope Plot simulation tool that allows the user to quickly predict the output delay response in the STANDALONE, FOLLOW or CONTROL modes. Figures 5 and 6 demonstrate ClockWizard's Scope Plot simulation capability.

DIRECT CLOCKING HIGH SPEED CONVERTERS WITH THE LTC6950

For high performance clocks, high speed ADCs are the de facto benchmark, due to their industry leading clock jitter requirements. There is a tremendous amount of literature that discusses requirements and recommendations for clocking high speed ADCs, but all can be summarized with the following statement: ADCs require a really low phase noise/jitter clock to meet signal to noise ratio (SNR) targets, and it is recommended that the ADC input clock is a differential clock and has fast clock edges.

Historically, these high speed ADC clocking requirements have been attainable, but only at high cost. This section shows the value of the LTC6950's ability to directly clock high speed ADCs, especially in regards to simplicity and performance.

ADC documents often start out with the following two equations.

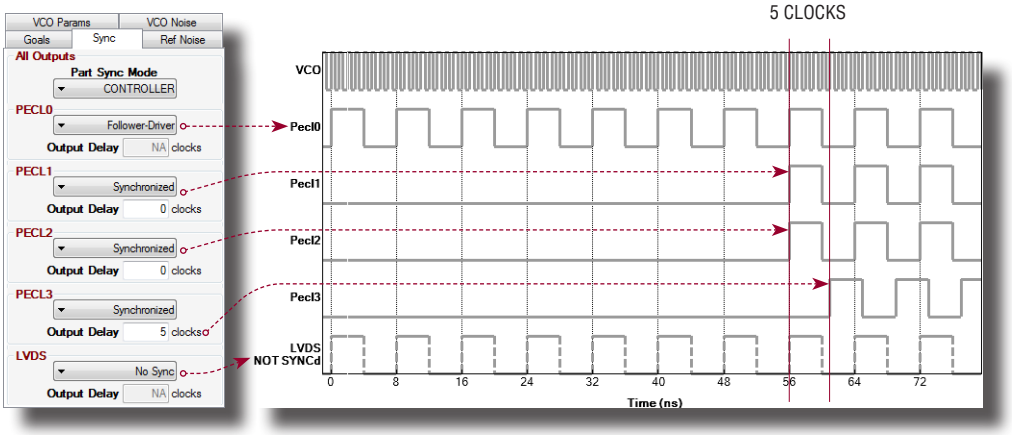
$$JITTER_{TOTAL} = \sqrt{(JITTER_{CLK\_IN})^2 + (JITTER_{APERTURE})^2} \quad (2)$$

$$SNR_{ADC} = 20 \bullet LOG \frac{1}{2\pi f_{IN} \bullet JITTER_{TOTAL}} \quad (3)$$

where f_{IN} = ADC analog input frequency

Equation 2 reminds the user the clock circuitry internal to the ADC also has jitter, known as aperture jitter. Most ADC data sheets provide a typical aperture jitter number for use with Equation 2. Equation 2 then states the

Figure 6. ClockWizard's Scope Plot tool shows simulated results of LTC6950 CONTROL mode



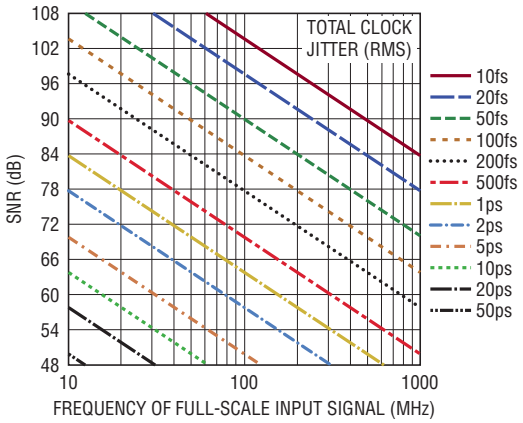


Figure 7. Graphical representation of Equation 3

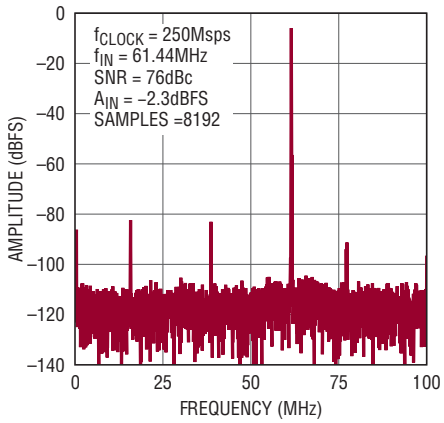


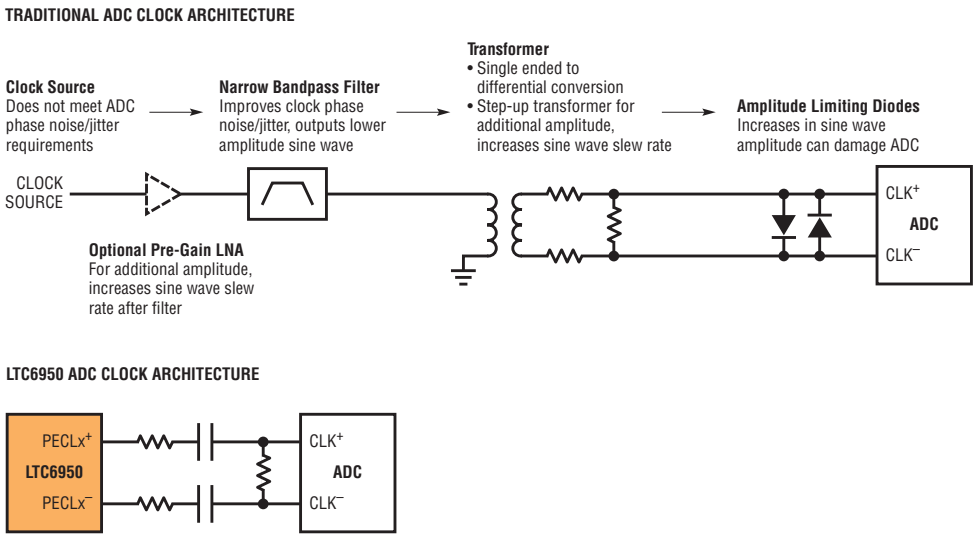
Figure 8. LTC6950 direct ADC clocking performance

ADC aperture jitter and the clock jitter at the input of the ADC add together in a square root of the sum of squares fashion to produce a total clock jitter.

Equation 3 relates total clock jitter to the ADC SNR performance. This equation is often best visualized by Figure 7. The main point to remember from Equation 3 is as the ADC input frequencies and SNR levels increase, the total clock jitter requirements become more stringent. It is worth clarifying that Equation 3 is dependent on the ADC's analog input frequency, not the clock frequency.

The LTC6950 achieves <100fs RMS jitter. Figure 8 is an SNR plot using the LTC2107 16-bit ADC at a f_{IN} = 61.44MHz (see Figure 8). Traditionally, to achieve this level of SNR performance from the ADC, additional onboard circuitry was needed to condition the clock signal. For example, in Figure 9, a single channel of a traditional ADC clock architecture is compared to a LTC6950 direct ADC clocking architecture. A single LTC6950 has four differential PECL channels that can drive four ADC clocks simultaneously. To drive four ADC clocks, the traditional clock architecture would repeat four times. As a result, the LTC6950 reduces design complexity, saves board space and lowers the cost of the overall board design.

Figure 9. Advantages of direct ADC clocking with the LTC6950



"All things are difficult before they are easy."
—Thomas Fuller

LTC6950 DESIGN AND SIMULATION EXAMPLE

ClockWizard is a tool that greatly simplifies the clock system design process. In addition to being able to read and write to the LTC6950's SPI registers, the ClockWizard includes a PLL loop filter design tool, a clock output divider/delay configuration tool, a phase noise simulation tool and a clock output timing simulation tool. A typical design for the LTC6950 utilizes the four differential PECL outputs to clock four data converters and the remaining LVDS/CMOS output to clock an FPGA. The following example highlights the ClockWizard design and simulation capabilities when designing a typical application circuit.

Designing the PLL

Download ClockWizard at www.linear.com/ClockWizard and install. The design presented here assumes use of the onboard VCO and reference that arrive installed on the LTC6950's demonstration circuit DC1795A. The values for these onboard components are pre-programmed into the ClockWizard under the VCO Params, VCO Noise and Ref Noise tabs shown in Figure 11. Using ClockWizard, enter the design goals and components required to complete the design, as shown in Figure 11.

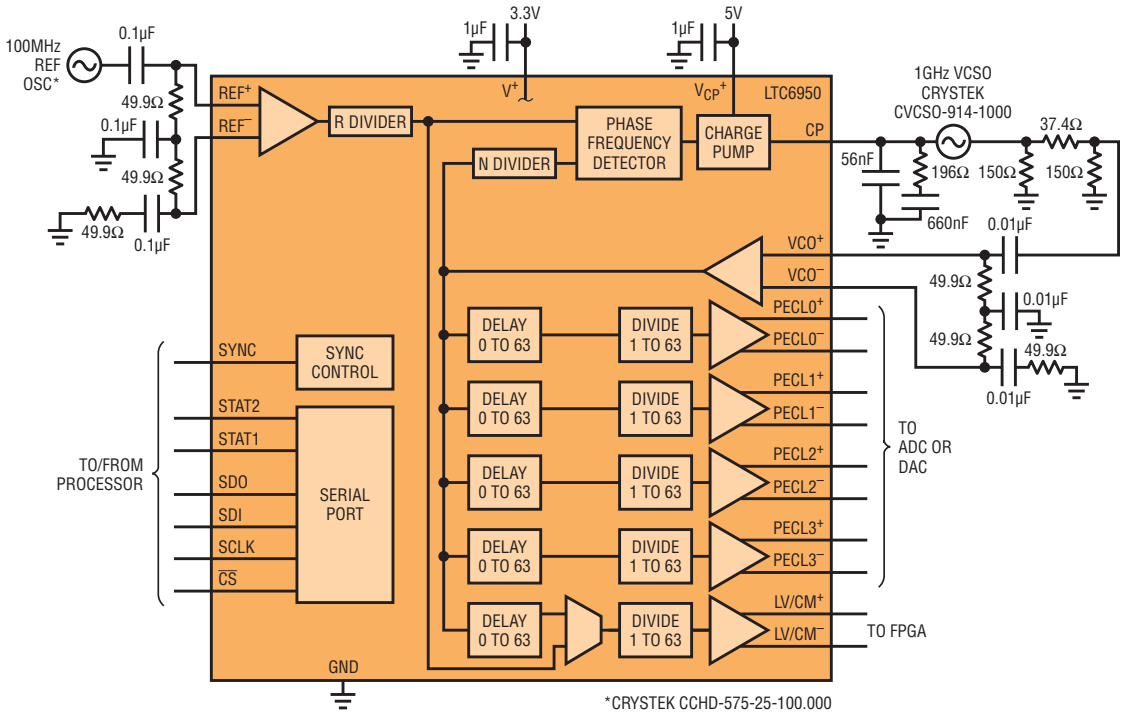
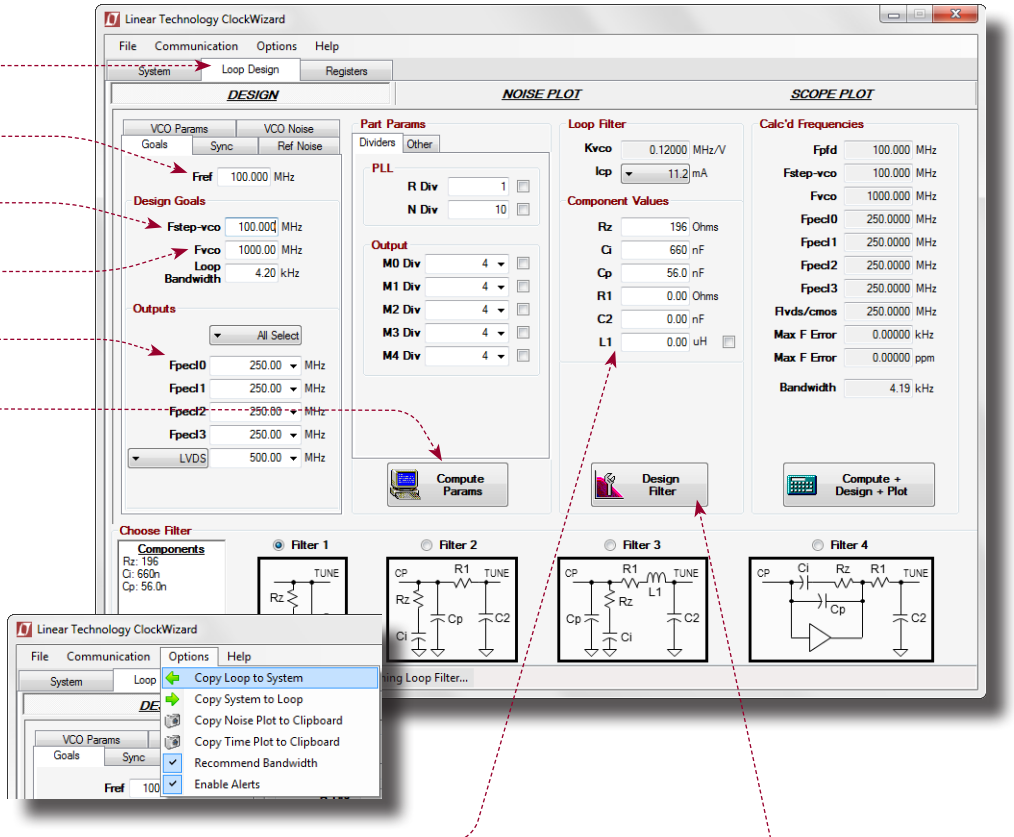


Figure 10. LTC6950 typical application

Figure 11. ClockWizard LTC6950 loop filter design

1. Select Loop Design
2. Enter reference frequency
3. Enter desired PFD frequency
4. Enter VCO frequency
5. Enter clock frequencies for each of the five clock outputs
6. Click Compute Params
7. Click Design Filter—Filter 1
8. Update component values with the practical component values shown
9. Choose Copy Loop to System from the Options menu. (This updates the System and Register Tab with the correct Serial Interface Values. If a demo board is connected, its serial interface registers are also updated.)



Simulating and Building the PLL

As shown in Figure 11, replace the filter components determined by ClockWizard with the nearest standard component values. In Figure 12, ClockWizard predicts the phase noise of the LTC6950 and the new loop filter for any of the five clock outputs selected in the noise plot. This plot shows how the VCO and reference phase noise affects the total noise, helping the designer choose the VCO and reference components. Once the output phase noise simulation meets the design goals, install the simulated loop filter values onto the DC1795A.

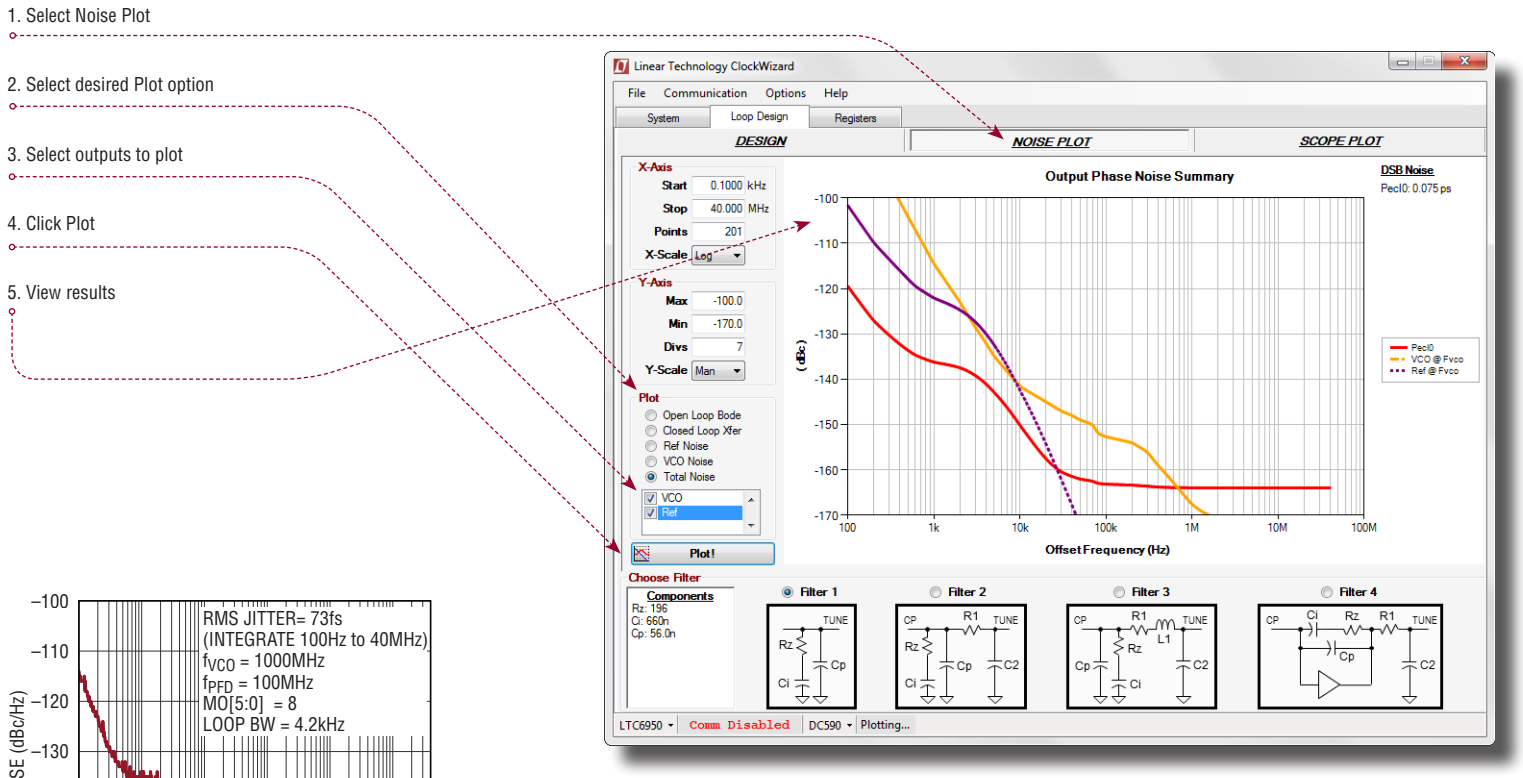
Evaluating the PLL

At this point the LTC6950 can be powered up and evaluated using the DC1795A. Download the DC1795A demonstration circuit manual at linear.com/product/LTC6950#demoboards and follow the power up instructions under the quick start procedure. Verify the output of this example by connecting one of the PECL outputs of the DC1795A to a signal source analyzer, such as Agilent's E5052. Figure 13 shows the measured result, which aligns closely with ClockWizard's simulated results in Figure 12.

CONCLUSION

The LTC6950 is the first device to offer Linear Technology's EZSync technology, which simplifies aligning multiple clocks across multiple parts, boards and systems. The LTC6950 performance levels enable direct clocking of high performance data converters, simplifying system design and reducing overall system cost. To further simplify the design process, ClockWizard was developed to design the loop filter, simulate phase noise and simulate clock output timing and cycle delays. ■

Figure 12. Simulating the LTC6950 loop filter performance using ClockWizard



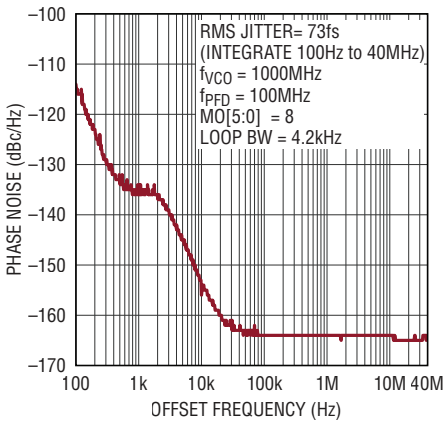


Figure 13. LTC6950 PECL0+ measured result at 125MHz

1.5A Monolithic Buck-Boost DC/DC Converter with Up to 95% Efficiency Features 2.5V–15V Input and Output Voltage Ranges

Richard Cook

Multicell high capacity batteries are increasingly becoming commonplace in handheld devices and industrial instruments that receive their power from a variety of sources. To maximize battery run time and support the variety of power sources, voltage regulators in multipower source systems must be able to maintain a constant output voltage even as the input voltage source resides above, below or equal to the output. This can be accomplished using two separate power converters with two controller ICs. A better solution is to use a single buck-boost DC/DC converter, which offers a smaller, simpler and more efficient design, attributes critically important in handheld devices.

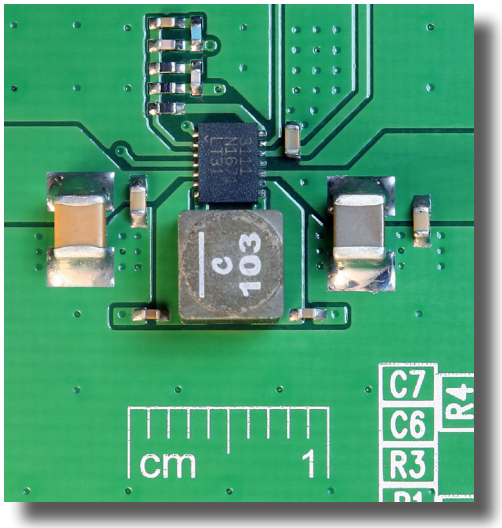
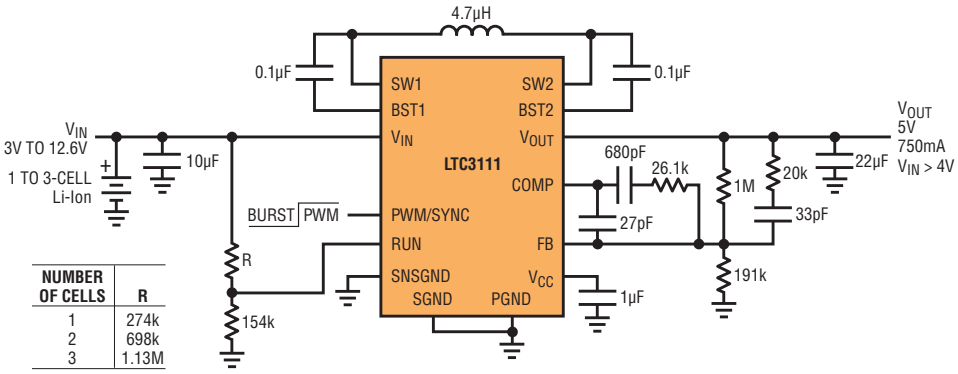


Figure 1. LTC3111-based 18W solution

The LTC3111 is a monolithic buck-boost converter with input and output voltage ranges of 2.5V to 15V and an output current capability of 1.5A. It allows conversion from a variety of power sources such as single or multi Li-ion cells, lead acid batteries, capacitor banks, USB cables or wall adapters.

In addition to its wide operating range, the LTC3111 features Linear Technology's proprietary low noise buck-boost PWM control architecture, effectively eliminating jitter and EMI that can occur when crossing the boundary between step-up and step-down operation. This reduces or eliminates the need for expensive filtering or shielding for noise sensitive data conversion or RF circuitry in the system. Selectable Burst Mode® operation extends the operating time when battery-powered devices are in idle by substantially reducing the quiescent current of the power converter.

Figure 2. One, two and three Li-ion cells can be used in this solution with the LTC3111's accurate RUN threshold feature



An accurate run threshold provides the ability to precisely program the turn-on threshold voltage of the converter. The integrated fault protection features include: current limit, thermal shutdown and short-circuit protection, which provides robust operation in harsh environments. For applications where component size is critical, the 800kHz default switching frequency can be synchronized up to 1.5MHz.

The LTC3111 based converter shown in Figure 1 can generate 18W of power with a 12V output. The solution footprint is less than 180mm², more compact than a controller-based buck-boost and much more efficient than a complex dual-inductor SEPIC converter design at similar power levels. The main external components are limited to the input, output filter capacitors and the power inductor. The LTC3111

In addition to its wide operating range, the LTC3111 features Linear Technology's proprietary low noise buck-boost PWM control architecture, effectively eliminating jitter and EMI that can occur when crossing the boundary between step-up and step-down operation. This reduces or eliminates the need for expensive filtering or shielding for noise sensitive data conversion or RF circuitry in the system.

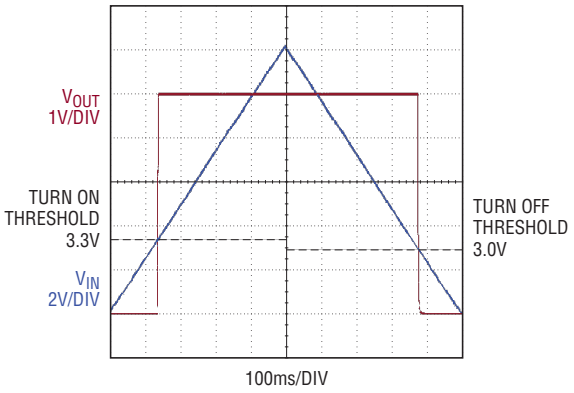


Figure 3. LTC3111 ramped input voltage response using the accurate run for a single Li-ion solution

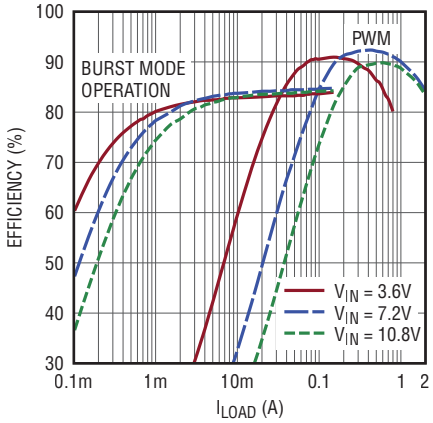


Figure 4. 5V output efficiency from one, two and three Li-ion cells

is offered in a thermally enhanced 16-lead 4mm × 3mm DFN or 16-lead MSOP package.

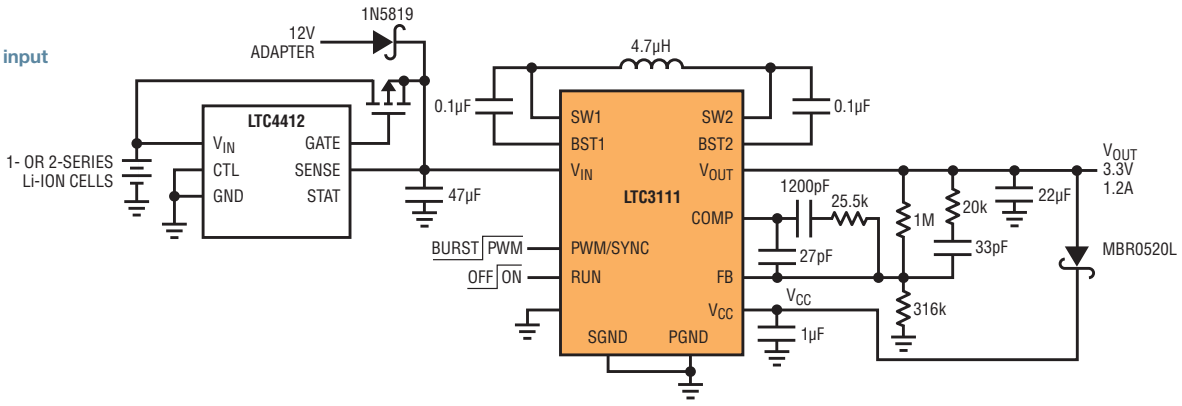
ACCURATE RUN THRESHOLD WITH 1-, 2- AND 3-CELL LI-ION

The LTC3111's RUN pin can either be used to enable/disable the converter via digital select, or to set an accurate user-programmable undervoltage lockout (UVLO) threshold—by a resistive divider from V_{IN} to ground. The LTC3111's RUN threshold of 1.2V (±5% over temperature) allows customization of the turn-on threshold voltage of the converter. Once enabled, 120mV of hysteresis is introduced at the RUN pin, requiring the source input voltage to drop 10% before disabling power conversion.

Figure 2 shows an application circuit where the accurate RUN pin threshold is used to turn the LTC3111 converter on/off when powered from a one, two or three Li-ion cell battery. For the single cell case, R is 267k, configuring the LTC3111 RUN pin to turn on when the input voltage is greater than 3.3V and to turn off when the input voltage drops below 3V.

This technique can be applied to two or three series cell designs by changing the value of R, as shown in the table for Figure 2. The output voltage response to a slowly ramped V_{IN} for the single cell case is shown in Figure 3. V_{OUT} in the single cell configuration turns on when the input voltage reaches 3.3V and turns off at 3V. Similarly, this plot can be scaled for 2- and 3-cell cases, where turn-on/

Figure 5. LTC4412 PowerPath™ controller selects highest voltage input to power the LTC3111 converter



The LTC3111 includes circuitry to minimize loop gain variation, resulting in improved line transient response. Regulation for V_{OUT} = 3.3V remains within 50mV, or 1.5%, during a 20µs, 7.2V-to-12V, V_{IN} rise and fall transition with a 22µF output capacitor and 1A load.

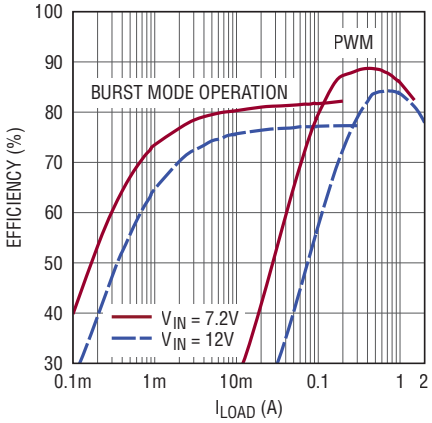


Figure 6. LTC3111 efficiency vs load current V_{OUT} = 3.3V, V_{IN} = 7.2V and 12V

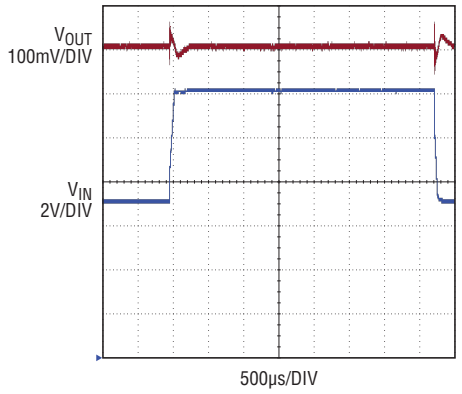


Figure 7. Line response for V_{OUT} = 3.3V, V_{IN} stepped from 7.2V to/from 12V

turn-off thresholds are 6.6V/6V and 9.9V/9V, respectively. The accurate RUN feature can also be applied to sources where operation must be restricted to a minimum input operating voltage such as a bank of capacitors, lead acid or NiCd batteries.

Efficiency curves for the one, two and three Li-ion cell designs operating at their typical voltages are shown in Figure 4. Peak efficiencies of greater than 90% are achieved over all three battery voltages. Note that the maximum load current capability for a 5V output decreases when the input voltage is less than 6V. The LTC3111 data sheet provides performance curves showing maximum output current capability versus input voltage in PWM and Burst Mode operation for various output voltages to aid in determining if the load can be supported over a specific input range.

MULTIPLE INPUT SOURCES

The wide operating range of the LTC3111 makes it easy to power devices from multiple input sources. Figure 5 shows an application where the LTC4412 PowerPath controller (SOT-23 package) selects from the higher of two input sources. The LTC4412 maintains a 20mV forward voltage across the selected P-channel MOSFET, keeping losses to a minimum. In this circuit, the LTC4412 switches the input of the LTC3111 to the greater of a 7.2V lithium ion battery or 12V wall adapter.

Efficiency curves versus load current for the 3.3V output, based on the two input sources, are given in Figure 6. Peak efficiencies of greater than 89% are achieved. Selectable Burst Mode operation with 49µA of typical sleep current extends high efficiency over two decades of load current.

The LTC3111 includes circuitry to minimize loop gain variation, resulting in improved line transient response. As illustrated in Figure 7, V_{OUT} regulation is maintained within 50mV, or 1.5%,

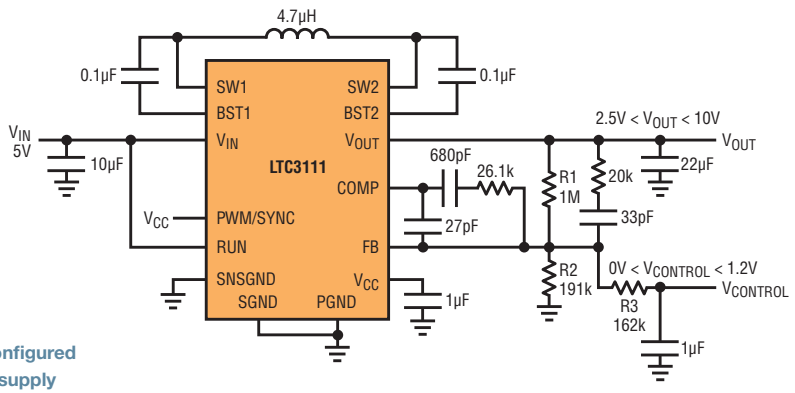


Figure 8. LTC3111 configured as a variable output supply

The LTC3111 provides low noise buck-boost conversion for a variety of applications requiring an extended input or output voltage range. The LTC3111's ability to support heavy loads makes it ideal for power hungry devices. Solution size and conversion efficiency benefit from the 90mΩ internal N-channel MOSFET switches and thermally enhanced packages.

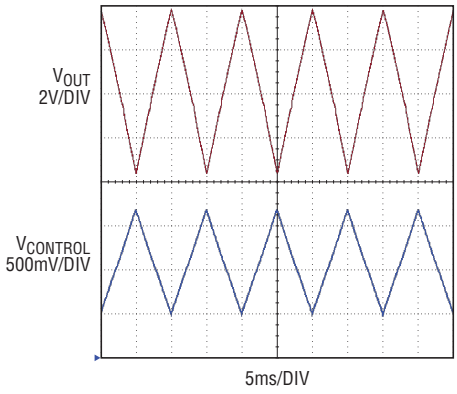


Figure 9. Variable output response using the LTC3111

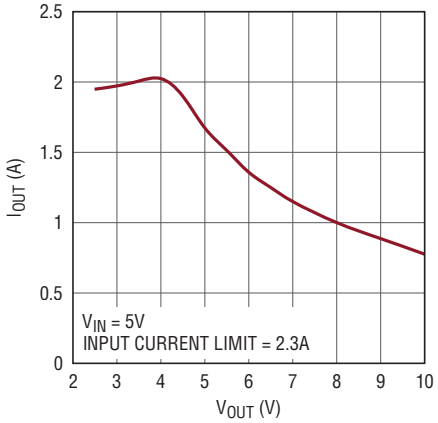


Figure 10. Maximum output current in PWM mode vs output voltage for V_{IN} = 5V

during the 20µs rise and fall transition with a 22µF output capacitor and 1A load in stepdown operation.

VARIABLE OUTPUT VOLTAGE USING THE LTC3111

For applications such as motor control, lighting or power supply margin testing, the LTC3111 can be configured as a variable voltage supply. This can be accomplished in a number of ways. Figure 8 shows one method: adding a summing resistor between the FB pin and a control voltage ($V_{CONTROL}$).

The programmed output voltage can be calculated using the following equation:

$$V_{OUT} = 0.8V\left(1+\frac{R1}{R2}\right)+\frac{R1}{R3}(0.8V-V_{CONTROL})$$

where R1 is the resistor connected between V_{OUT} and FB, R2 is the resistor connected from FB and ground and R3 is the resistor connected from FB and $V_{CONTROL}$.

Figure 9 shows the output voltage response of a 0V to 1.2V ramped control signal operating at 100Hz. The corresponding output voltage swings from 10V to 2.5V, providing an inverting gain of 6.2 from $V_{CONTROL}$ to V_{OUT}. The low noise PWM control provides low distortion and high quality replication of the input signal.

When using the LTC3111 as a variable output voltage regulator, the maximum load current capability of the LTC3111 is reduced when $V_{OUT} > V_{IN}$ (i.e., when the part is in boost or step-up mode). As Figure 10 shows, the maximum output current capability is effectively reduced by the step-up ratio of the converter.

For example, the output current capability when $V_{OUT} = 2V_{IN}$ is roughly one half the capability when $V_{OUT} = V_{IN}$. In the example application above, a fixed 500mA load is applied to the output, which the part is capable of supplying at all output voltages. To ensure converter stability, compensation values for this application are determined at the highest boost ratio of V_{IN} = 5V to V_{OUT} = 10V.

SUMMARY

The LTC3111 provides low noise buck-boost conversion for a variety of applications requiring an extended input or output voltage range. The LTC3111's ability to efficiently support heavy load currents makes it ideal for power hungry devices. Solution size and conversion efficiency benefit from the 90mΩ internal N-channel MOSFET switches and thermally enhanced packages. Low quiescent current Burst Mode operation extends high efficiency over several decades of load current, enabling longer run times in many battery powered applications. ■

Hundreds of Watts, 60V In or Out: Synchronous 4-Switch Buck-Boost Converter is Easy to Parallel to Minimize Temperature Rise

Keith Szolusha

The LT3790 is a 4-switch synchronous buck-boost DC/DC converter that regulates both constant voltage and constant current at up to 98.5% efficiency using only a single inductor. It can deliver hundreds of watts and features a 60V input and output rating, making it an ideal DC/DC voltage regulator and battery charger when both step-up and step-down conversion are needed.

A single LT3790 converter can deliver high power due to its synchronous switching topology, but eventually the switching and/or conduction losses at higher power can overwhelm a single converter with excessive board heating. Although heat can be mitigated with bulked up heat sinks, additional external gate drivers, and/or forced airflow, it may be better to simply tie together two or more converters in parallel to spread the load. This is easy to do with the LT3790 buck-boost regulator.

120W, 24V, 5A OUTPUT BUCK-BOOST VOLTAGE REGULATOR

The buck-boost converter shown in Figure 1 regulates 24V with 0A–5A load at up to 98.5% efficiency. It operates from an input voltage range of 8V to 56V. Adjustable undervoltage and overvoltage lockout protect the circuit. It has short-circuit protection and the $\overline{\text{SHORT}}$ output flag indicates when there is a short circuit on the output. It features DCM operation at light load for lowest power consumption and reverse current protection. The sense resistor R_{OUT} sets the output current limit during

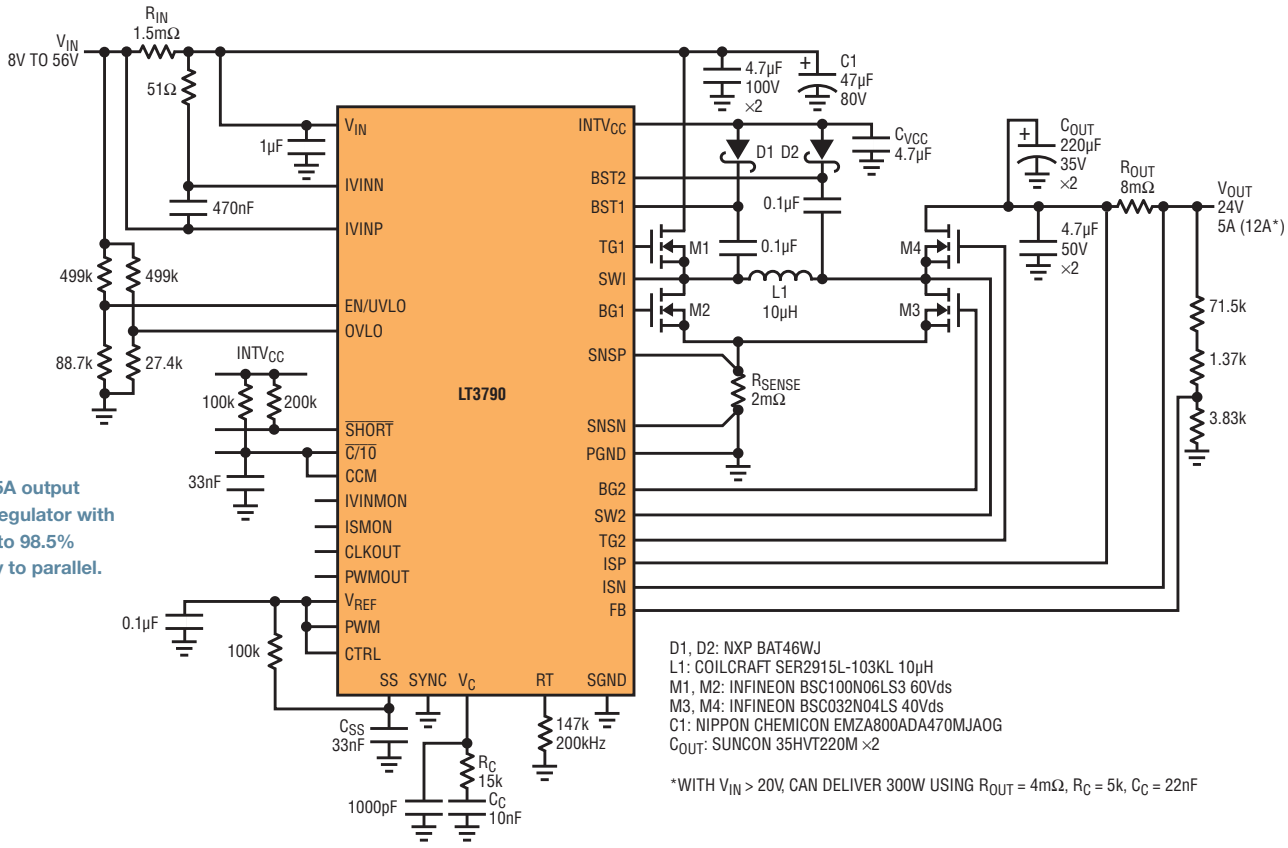
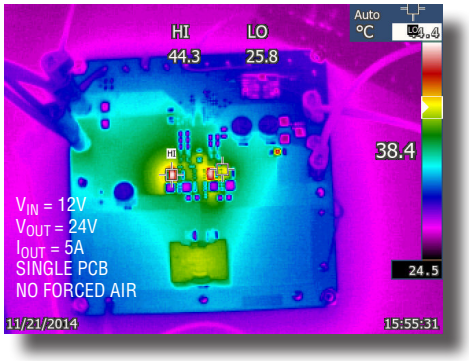


Figure 1. 120W, 24V, 5A output buck-boost voltage regulator with 8V–56V input has up to 98.5% efficiency and is easy to parallel.

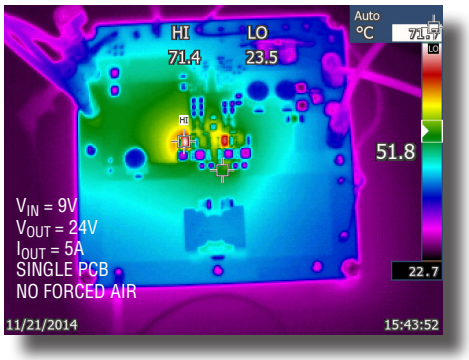
D1, D2: NXP BAT46WJ
L1: COILCRAFT SER2915L-103KL 10µH
M1, M2: INFINEON BSC100N06LS3 60Vds
M3, M4: INFINEON BSC032N04LS 40Vds
C1: NIPPON CHEMICON EMZA800ADA470MJAOG
C_{OUT}: SUNCON 35HVT220M ×2

*WITH V_{IN} > 20V, CAN DELIVER 300W USING R_{OUT} = 4mΩ, R_C = 5k, C_C = 22nF

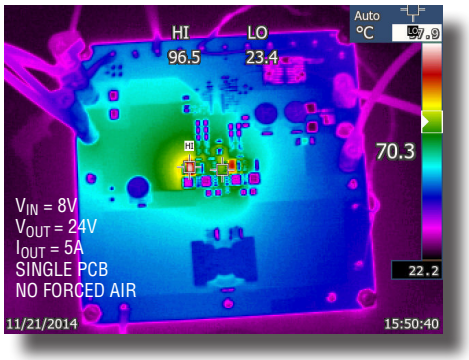
Figure 2. Single 24V, 5A converter shown in Figure 1 has a maximum of 20°C temp rise on any component at 12V input (a) and 50°C at 9V input (b). Even at 8V input (c), the hottest component reaches only 96.5°C without forced airflow or heat sinking.



(a)

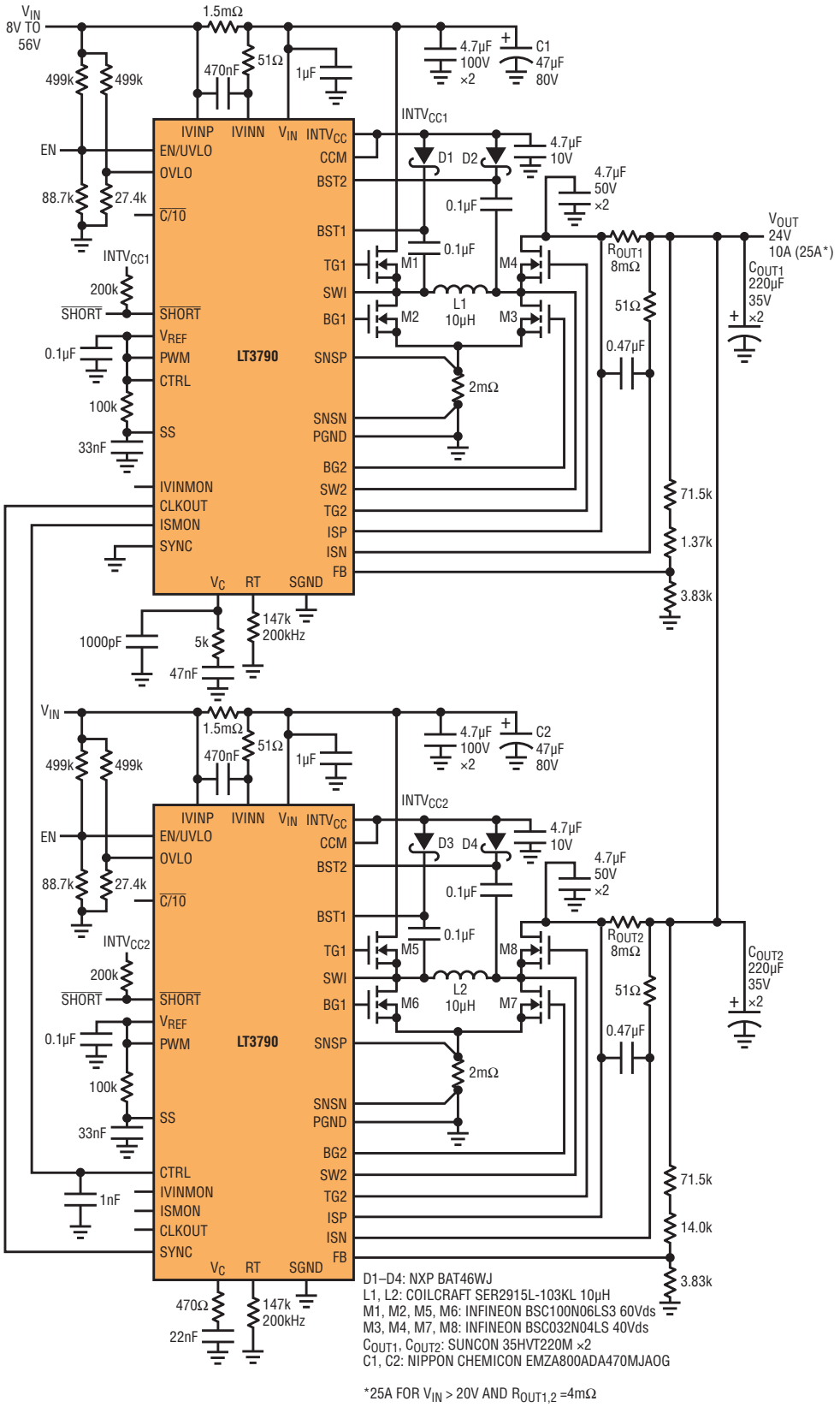


(b)



(c)

Figure 3. Two LT3790 24V voltage regulators are easy to parallel for double the output with limited discrete component temperature rise.



The CLKOUT pin of the master can be directly tied to the SYNC input pin of the slave for 180° phase-interleaving of the two parallel converters. The 180° phase difference between the converters reduces overall converter output ripple, instead of doubling it. If more than two converters are connected in parallel, they can be synchronized to either operate phase-shifted or in-phase with an external clock source, or daisy-chaining CLKOUT pins.

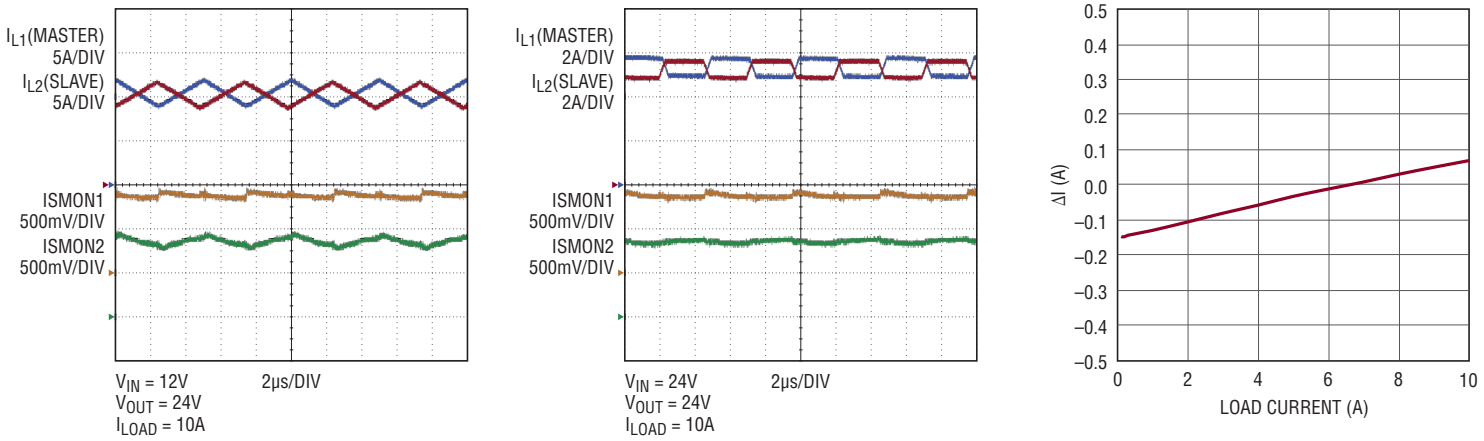


Figure 4. Parallel converter inductor and output current matching

both a short-circuit and overload situations, making this a robust application.

The temperature rise of this 120W board at 12V input is only 20°C on the hottest component (a switching MOSFET) as shown in Figure 2a. There is still margin for either higher output power at 12V input, or the same 120W from a lower V_{IN} without excessive component temperature rise—note that higher output power requires a correspondingly increased output current limit. When operated down to 8V input with 120W output, the components on this standard 4-layer LT3790 PCB remain below 97°C (at room temp) without forced airflow or heat sinking. To deliver significantly higher power with the same, limited temperature rise and input voltage range, two or more LT3790 converters can easily be connected in parallel.

PARALLEL CONVERTERS, CONSTANT VOLTAGE MASTER, CONSTANT CURRENT SLAVE

Ideally, paralleled switching converters share the load equally throughout the entire output range. The LT3790's ability to run in either constant voltage or constant current operation allows one master converter to control the output voltage, while its current monitor output (ISMON) tells one or more slave converters how much output current to regulate (CTRL input) in order to match its own output level. Current matching between multiple converters is nearly ideal using this technique.

The CLKOUT pin of the master can be directly tied to the SYNC input pin of the slave for 180° phase-interleaving of the two parallel converters. The 180° phase difference between the converters reduces overall converter output ripple, instead of doubling it. If more than two converters are connected in parallel, they can be synchronized to either operate phase-shifted or in-phase with an external clock source, or daisy-chaining CLKOUT pins.

Figure 3 shows a 24V, 10A (or 25A under certain conditions, see figure) voltage regulator formed by running two LT3790s in parallel. By using two parallel circuits, the maximum temperature rise on any one discrete component is only 20°C for the M3 and M7 MOSFETs at 12V input and 50°C at 9V input.

The top converter (master) in Figure 3 regulates the 24V output voltage and commands the current level that is regulated by the bottom (slave) converter. The ISMON output of the master indicates how much current the master is providing, and by connecting ISMON directly to the CTRL input of the slave, the slave is forced to follow the master. The LT3790 ISMON output level and CTRL input level are identically mapped so that a direct connection from one to the other is possible, and doing so forces the total output current to be shared equally between the

Ideally, paralleled switching converters share the load equally throughout the entire output range. The LT3790's ability to run in either constant voltage or constant current operation allows one master converter to control the output voltage, while its current monitor output (ISMON) tells one or more slave converters how much output current to regulate (CTRL input) in order to match its own output level.

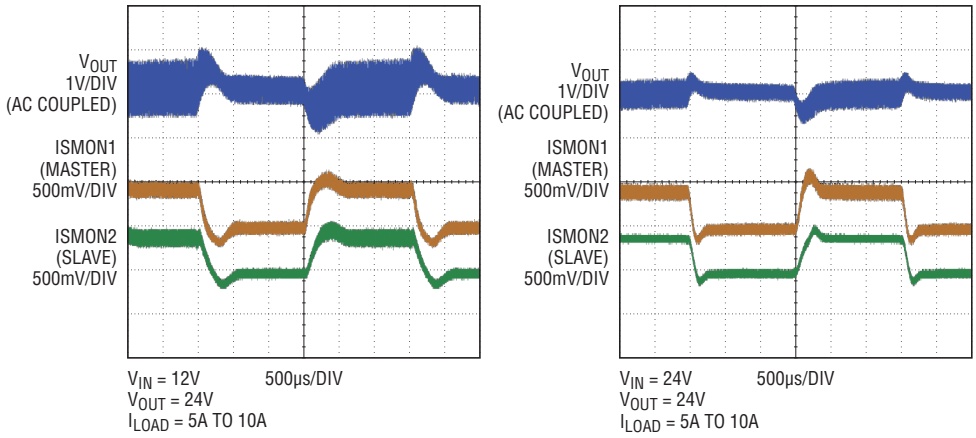


Figure 5. Parallel converter transient response evenly shares current

parallel converters, as shown in Figure 4. Note that the output voltage of the slave is set slightly higher (28V) so that the voltage feedback loop of the slave is not in regulation, allowing it to follow the master.

LOOP ANALYSIS FOR STABILITY

Transient response and network analyzer loop analysis can be used to measure stability. A transient response of 50% to 100% current, shown in Figure 5, demonstrates a properly compensated converter and equally shared load current. Further analysis with the network analyzer gives us the details of the separate converters. The noise injection point and measurement to generate control loop bode plots is different for the constant voltage regulator master and the constant current regulator slave. Separately, each loop can be measured by injecting the perturbation signal and measuring the loop response, as shown in Figure 6.

The constant current slave must have its loop broken and signal injected in the current loop feedback path instead of the traditional voltage feedback path since that is the feedback loop in use during parallel operation. The master bode plot in Figure 7 demonstrates the stability of the system.

CONCLUSION

The LT3790 synchronous buck-boost controller delivers over 100W at up to 98.5% efficiency to a variety of loads, and it is easy to parallel multiple converters for even higher power outputs. The ability to control either output voltage or current, combined with the level-matching of the ISMON output amplifier and the CTRL input amplifier, simplifies the connection of a master voltage regulator and one or more slave current regulators. The result is high power 60V buck-boost regulation that can deliver hundreds of watts at high efficiency. ■

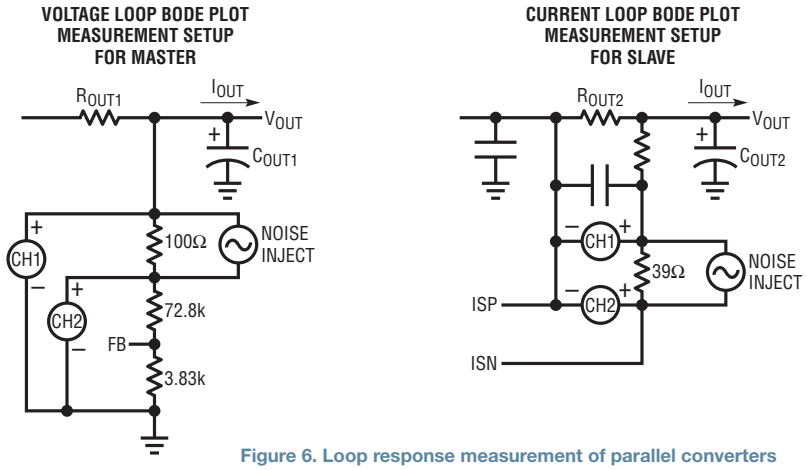


Figure 6. Loop response measurement of parallel converters

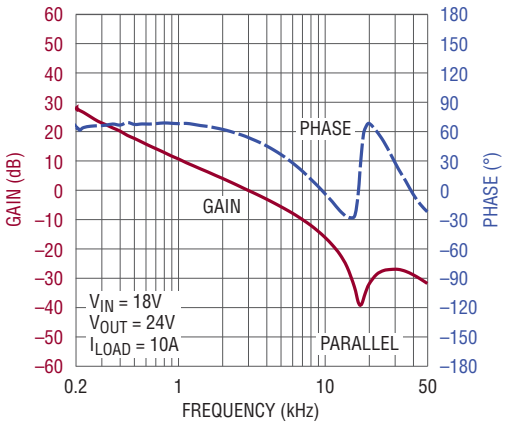


Figure 7. Bode plot shows measured results for parallel system.

What's New with LTspice IV?

Gabino Alonso

New Blog Video: "LTspice: SOAtherm Tutorial" by Dan Eddleman
www.linear.com/solutions/5445

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BLOG BY ENGINEERS, FOR ENGINEERS

Check out the LTspice blog (www.linear.com/solutions/LTspice) for tech news, insider tips and interesting points of view regarding LTspice.

New Video: "LTspice: SOAtherm Tutorial" by Dan Eddleman www.linear.com/solutions/5445

This video shows how to use the new SOAtherm models distributed with LTspice. SOAtherm models can be used to verify that the MOSFET maximum die temperature is not exceeded, even in the Spirito region, where allowable current falls off exponentially at high drain-to-source voltages. SOAtherm reports the temperature of the hottest point on the MOSFET die; SOAtherm models do not influence the electrical behavior of the circuit simulation.

What is LTspice IV?

LTspice® IV is a high performance SPICE simulator, schematic capture and waveform viewer designed to speed the process of power supply design. LTspice IV adds enhancements and models to SPICE, significantly reducing simulation time compared to typical SPICE simulators, allowing one to view waveforms for most switching regulators in minutes compared to hours for other SPICE simulators.

LTspice IV is available free from Linear Technology at www.linear.com/LTspice. Included in the download is a complete working version of LTspice IV, macro models for Linear Technology's power products, over 200 op amp models, as well as models for resistors, transistors and MOSFETs.

SELECTED DEMO CIRCUITS

For a complete list of example simulations utilizing Linear Technology's devices, please visit www.linear.com/democircuits.

Buck Regulators

- **LT8302:** Negative to negative buck converter (–18 to –42V, –12V 1.8A) www.linear.com/LT8302
- **LT6110/LT3976:** Buck regulator with cable/wire voltage drop compensation (5V–40V to 3.3V at 5A) www.linear.com/LT6110
- **LTC3639:** High efficiency, 150V synchronous buck converter (4V–150V to 3.3V at 100mA) www.linear.com/LTC3639
- **LTC3774:** High efficiency 2-phase buck converter with discrete MOSFET drivers (7V–14V to 1.2V at 60A) www.linear.com/LTC3774
- **LTC3838-1:** High current, dual output synchronous buck converter (4.5V–14V to 1.5V & 1.2V at 20A) www.linear.com/LTC3838-1
- **LTC3869:** high efficiency dual 1.5V/1.2V buck converter using DCR current sensing (4.5V–14V to 1.5V & 1.2V at 15A) www.linear.com/LTC3869
- **LTM4634:** Triple 5A/5A/4A µModule buck regulator (4.8V–28V to 1.0V, 3.3V at 5A & 12.0V at 4A) www.linear.com/LTM4634
- **LTM4639:** High efficiency 20A µModule buck regulator (2.4V–7V to 1.2V at 20A) www.linear.com/LTM4639

Boost Regulators

- **LT3048-15:** Low noise bias voltage generator from single cell Li-ion battery (2.7V–4.8V to 15V at 24mA) www.linear.com/LT3048-15
- **LTC3872:** High efficiency 5V input, 24V output boost converter (3V–9.8V to 24V at 1A) www.linear.com/LTC3872

Buck-Boost Converter

- **LT8302:** Negative to positive buck-boost converter (–4 to –42V V_{IN} to 12V V_{OUT} at 1.3A) www.linear.com/LT8302

Isolated Converters

- **LT8310:** 72W isolated nonsynchronous forward converter with opto feedback (36V–72V to 12V at 6A) www.linear.com/LT8310
- **LTM8058:** Series-conntected low noise isolated µModule regulators (5V–28V to 10V at 300mA) www.linear.com/LTM8058

SCAP Charger

- **LTC3625:** Solar powered SCAP charger with MPPT www.linear.com/LTC3625

Hot Swap Controller

- **LTC4226:** Dual 12V, 7.6A dual ideal diode and Hot Swap controller www.linear.com/LTC4226
- **LTC4232:** 12V, 5A Hot Swap controller with auto-retry www.linear.com/LTC4232

VOLTAGE CONTROLLED SWITCHES

LTspice includes a large number of excellent FET models, but sometimes you need to simulate a simple switch that opens and closes at specific times or under certain conditions.

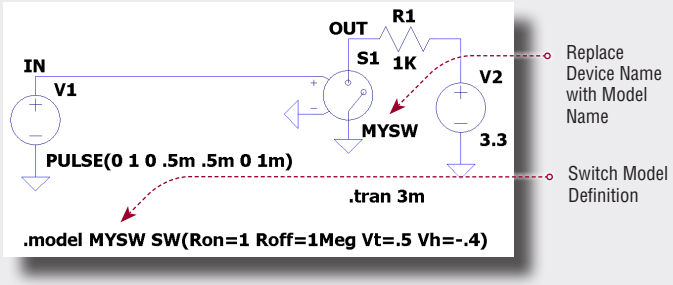
To insert and configure a switch in LTspice… (This example is available in LTspice at \LTspiceIV\examples\Educational\Vswitch.asc)

1. Insert the symbol for the voltage-controlled switch in your schematic (press F2 and type "sw" in the search field of the symbol library).
2. Insert a SPICE directive (press S) and define the SW model's parameters using this example:

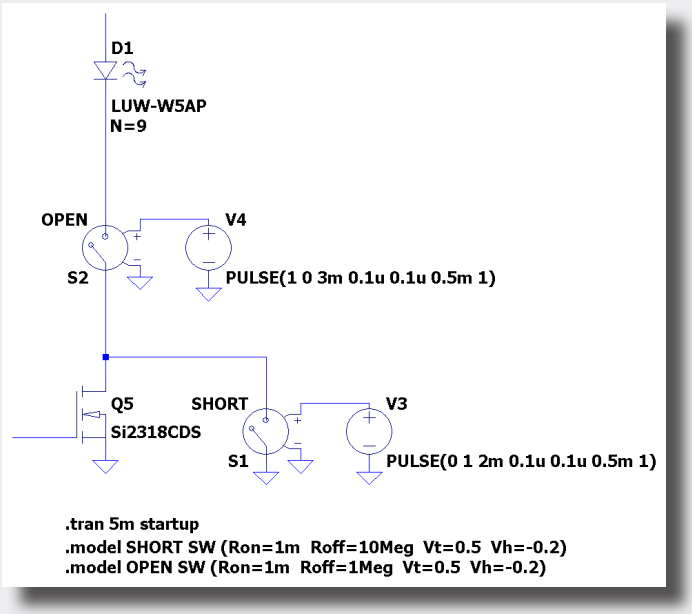
   `.model MYSW SW(Ron=1 Roff=1Meg Vt=.5 Vh=-.4)`

   where "MYSW" is the unique model name, Ron and Roff are the on and off resistances and Vt and Vh are the trip and hysteresis voltages. The switch trips at (Vt – Vh) and (Vt + Vh).

   LTspice Help (press F1) contains more about the SW model parameters.
3. Assign the MYSW model to the switch symbol S1: right-click "SW" and enter the unique model name, "MYSW".
4. Control the switch with a voltage source connected to the positive terminal of the switch and ground the negative terminal. In this example a PULSE function source is used to generate a 0V–1V triangle waveform with a 1ms period.



One classic application of voltage-controlled switches is simulating open-circuit and short-circuit conditions. In the example shown, two switches simulate a short- and open-circuit condition on an LED string.



Happy simulations!

Power User Tip

SELECT MODELS

To search the LTspice library for a particular device model, choose Component from the Edit menu or press F2. LTspice is updated often with new models, so be sure to keep your installation of LTspice current by choosing Sync Release from the Tools menu. LTspice's changelog.txt file (in the root installation directory) lists the LTspice revision history.

Buck Regulators

- **LTC3637:** 76V, 1A step-down regulator www.linear.com/LTC3637
- **LTM4639:** Low V_{IN} 20A DC/DC µModule step-down regulator www.linear.com/LTM4639

Boost Regulators

- **LTC3124:** 15V, 5A 2-phase synchronous step-up DC/DC converter with output disconnect www.linear.com/LTC3124

Buck-Boost Regulators

- **LT3790:** 60V synchronous 4-switch buck-boost controller www.linear.com/LT3790 www.linear.com/LT3790

Forward Controllers

- **LT3752-1:** Active clamp synchronous forward controllers with internal housekeeping controller www.linear.com/LT3752

Battery Management/Chargers

- **LT8584:** 2.5A monolithic active cell balancer with telemetry interface www.linear.com/LT8584
- **LTC4054-4.2:** Standalone linear Li-ion battery charger with thermal regulation www.linear.com/LTC4054-4.2
- **LTC4079:** 60V, 250mA linear charger with low quiescent current www.linear.com/LTC4079

Precision Amplifiers

- **LT6017:** Quad 3.2MHz, 0.8V/µs low power, Over-The-Top® precision op amp www.linear.com/LT6017
- **LTC6268/LTC6269:** Single/dual 500MHz ultralow bias current FET input op amp www.linear.com/LTC6268

High Speed Comparators

- **LTC6752:** 280MHz, 2.9ns comparator family with rail-to-rail inputs and CMOS outputs www.linear.com/LTC6752 ■

Analysis of Hot Swap Circuits with Foldback Current Limit

Vladimir Ostrerov and Josh Simonson

A reliable analog circuit guarantees proper operation within the parametric tolerances of the active controlling IC and passive components. For a Hot Swap circuit to perform properly, the minimum and maximum values of a number of parameters must be gathered from the data sheets of all components. From these, the Hot Swap circuit's behavior in the face of various capacitive loads should be known. This article shows how critical capacitive loads are calculated for Hot Swap circuits with foldback current limit characteristics.

OVERVIEW

For a Hot Swap circuit, as shown in Figure 1, the critical parameters are operating voltage (V_{OPER}) maximum current limit (I_{LIMIT}) timer period (T) and the maximum output voltage slew rate (S_O), which happens when the Hot Swap circuit starts to operate with no-load. These parameters are selected initially based on the load requirements, supply limitations and MOSFET's drain-source on-resistance ($R_{DS(ON)}$) and its safe operating area (SOA).

While slewing, the MOSFET acts as a source follower so the maximum output voltage slew rate, S_O, is the same as the GATE pin slew rate S_G, and it is defined by the circuit components (gate current divided by gate to ground capacitance), and has a strong influence on the power up transient. The timer period, T, is the time allowed for the Hot Swap circuit to operate in current limit mode before a fault is generated. A successful power-up transient is one that does not generate a fault.

The problem of proper operation over the full variation of the circuit parameters is relatively simple for a circuit with constant current limit, I_{LIMIT}. The relationship of parameters of a purely capacitive load at the constant current limit for time T is:

$$C_{LOAD} = \frac{I_{LIMIT} \bullet T}{V_{OPER}}$$

For an R-C load it is easy to define a surplus current, which is allowed for the capacitive component of the load, and select proper load capacitance.

There are two common problems that require solutions when charging a load with a Hot Swap circuit:

- The maximum pure capacitive load for a successful power-up transient.
- The maximum capacitive load, which can be added in parallel to a resistive load, R_L, for a successful power-up transient.

A linear approximation of the foldback characteristic is shown in Figure 1b. It is used in all the following considerations. The main points of this characteristic are:

- The operating voltage is V_{OPER}.
- The initial current limit value, when the output voltage $0 \le V_{OUT} \le V_{INIT}$, is I_{INIT}.

This current limit value persists until the output voltage reaches V_{LIMIT} (point A), after which the current limit increases linearly, which occurs after the output voltage reaches V_{FIX} (point B). After point B the current limit is constant (I_{LIMIT} = constant). The voltage V_{FIX} is lower than V_{OPER}.

The current limit value as a function of the output voltage, shown in Figure 1b, is expressed by three separate equations for different output voltage levels:

$$\begin{Bmatrix} I_{LOAD}(V_{OUT}) = I_{INIT} \\ \text{when} \\ 0 \le V_{OUT} \le V_{INIT} \end{Bmatrix} \quad (1)$$

$$\begin{Bmatrix} I_{LOAD}(V_{OUT}) = I_{INIT} + \alpha \bullet V_{OUT}(t) \\ \text{when } V_{INIT} \le V_{OUT} \le V_{FIX} \\ \text{where } \alpha = \dfrac{I_{LIMIT} - I_{INIT}}{V_{FIX} - V_{INIT}} \end{Bmatrix} \quad (2)$$

$$\begin{Bmatrix} I_{LOAD}(V_{OUT}) = I_{LIMIT} \\ \text{when} \\ V_{FIX} \le V_{OUT} \le V_{OPER} \end{Bmatrix} \quad (3)$$

The value of the parameters marked on Figure 1b, the timer period T value and the slew rate S_O are all known, with tolerance, and used in the following solutions. For some circuits, the slew rate S_O is fast enough that it has a negligible effect on the inrush transient, and for others, it is significant. The two loads above are solved for these two cases of slew rate.

CALCULATING THE MAXIMUM PURE CAPACITIVE LOAD

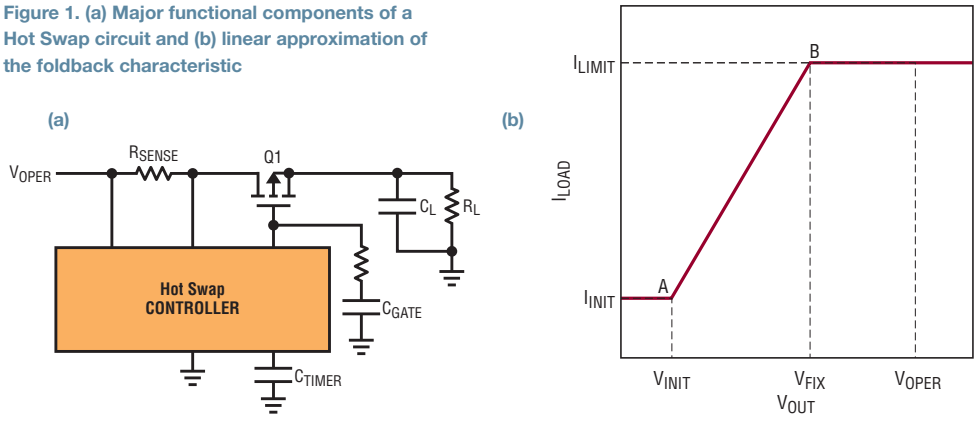
One important parameter to know for a Hot Swap circuit is the maximum pure capacitive load that a circuit can successfully power up into without a fault.

Consider two critical capacitive loads: C_{NO_FLT} and C_{FLT}. C_{NO_FLT} is the maximum capacitive load with which the circuit passes the power-up transient without a fault for any possible combination of circuit parameters. C_{FLT} is the minimum capacitive load with which the power-up transient is always unsuccessful, and a fault is generated. From these, the capacitive load range can be divided into three groups. The power-up transient is successful for capacitive loads from zero to C_{NO_FLT}. Power-up is unsuccessful for loads larger than C_{FLT}. The power-up transient is unpredictable for loads from the C_{NO_FLT} to C_{FLT}.

The following Hot Swap circuit parameters can be initially defined with tolerance: V_{INIT}, V_{FIX}, I_{INIT}, I_{LIMIT}, T.

The function $I_{LOAD}(V_{OUT})$ shown in Figure 1b and equations (1–3) has three distinct operating regions for current limit. The slew rate, S_O, can either cause the circuit to leave a current limit mode in any of these operating regions (before the timer period T expires), or it can have no effect (i.e., S_O is very fast). Each of these scenarios, transients, should by analyzed for any Hot Swap circuit. Each is described below. Some transients allow finding an analytical expression for the worst-case parameters.

Figure 1. (a) Major functional components of a Hot Swap circuit and (b) linear approximation of the foldback characteristic



However, the general or universal solution can be obtained in a numerical form.

Case 1: S_O Never Limits Current

Suppose that natural slew rate S_O is fast enough to keep the operating point in current limit mode in all three portions of the function $I_{LOAD}(V_{OUT})$.

In the first stage of the transient, the current is I_{INIT} and the output voltage rises linearly from zero to V_{INIT} during the time t_1. The capacitive load C_{LOAD1} can be expressed as:

$$C_{LOAD1} \le \frac{I_{INIT} t_1}{V_{INIT}} \quad (4)$$

In the second stage of the transient, the current increases linearly from I_{INIT} to I_{LIMIT} according to (2) as the output voltage increases from V_{INIT} to V_{FIX}. Time t_2 represents the duration of this stage, completed when the output voltage reaches V_{FIX}. V_{FIX} is usually set to (0.5 to 0.9)V_{OPER} (it must be lower than V_{OPER}) by proper selection of the resistive divider.

The output voltage as a function of time is:

$$V_{OUT}(t) = \frac{1}{C_{LOAD1}} \int_0^{t1} I_{LOAD}(t)\,dt \quad (5)$$

Substituting the expression (2) in equation (5) produces:

$$V_{OUT}(t) = \frac{1}{C_{LOAD1}} \int [I_{INIT} + \alpha \bullet V_{OUT}(t)]\,dt \quad (6)$$

or

$$\frac{dV_{OUT}(t)}{dt} = \frac{I_{INIT} + \alpha \bullet V_{OUT}(t)}{C_{LOAD1}} \quad (7)$$

which leads to the first order differential equation

$$\frac{dV_{OUT}(t)}{dt} - \frac{\alpha}{C_{LOAD1}} \bullet V_{OUT}(t) - \frac{I_{INIT}}{C_{LOAD1}} = 0 \quad (8)$$

with initial condition

$$V_{OUT}(0) = V_{INIT} = \frac{I_{INIT} t_1}{C_{LOAD1}} \quad (9)$$

Equation (8) describes $V_{OUT}(t)$ from the start of stage 2, t = 0, to time t_2, when the current limit reaches its maximum value, I_{LIMIT}.

The solution for Equation (8) is:

$$V_{OUT}(t) = \left(\frac{I_{INIT}}{\alpha} + V_{INIT}\right) e^{(\alpha t / C_{LOAD1})} - \frac{I_{INIT}}{\alpha} \quad (10)$$

The output voltage at time t_2 is V_{FIX}

$$V_{OUT}(t_2) = V_{FIX} =$$
$$= \left(\frac{I_{INIT}}{\alpha} + V_{INIT}\right) e^{(\alpha t_2 / C_{LOAD1})} - \frac{I_{INIT}}{\alpha} \quad (11)$$

The duration of interval t_2 is

$$t_2 = \left(\frac{C_{LOAD1}}{\alpha}\right) \bullet \ln\left(\frac{V_{FIX} + \frac{I_{INIT}}{\alpha}}{V_{INIT} + \frac{I_{INIT}}{\alpha}}\right) \quad (12)$$

The third equation should describe how C_{LOAD1} is charged with current I_{LIMIT} during the interval t_3 from V_{FIX} to some intermediate-level $V_{INTERIM}$ where the

There are two common problems that require solution when charging a load with a Hot Swap circuit: (1) the maximum pure capacitive load for a successful power-up transient; and (2) the maximum capacitive load, which could be added in parallel to a resistive load, R_L, for a successful power-up transient.

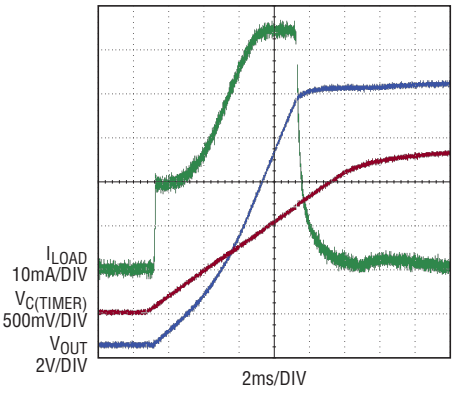


Figure 2. (Case 1) Pure capacitive load. Operating point leaves current limit mode in the third area, where current limit is I_{LIMIT}.

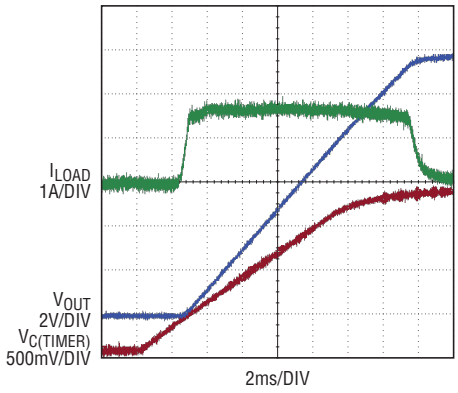


Figure 3. (Case 2) Pure capacitive load with a limited S_O (natural output voltage slew rate). Operating point leaves current limit mode in the first area, where current limit is I_{INIT}.

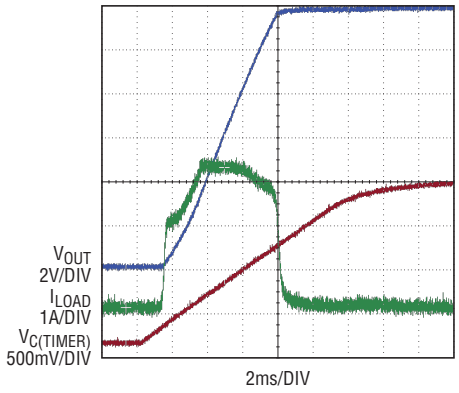


Figure 4. (Case 4) Pure capacitive load with a limited S_O (natural output voltage slew rate). Operating point leaves current limit mode in the second area, where current limit rises linearly.

operation point leaves a current limit mode because the MOSFET transconductance drops off in the triode region. When this region is entered, successful start-up is assured, but the point at which this region begins is difficult to solve for because it involves MOSFET parameters that may not be available. This region is usually small, so it makes sense to simplify the description of this region with the assumption that C_{LOAD1} is charged from V_{FIX} to V_{OPER} with I_{LIMIT}. In this case the time:

$$t_3 = \frac{C_{LOAD1}(V_{OPER} - V_{FIX})}{I_{LIMIT}} \quad (13)$$

according to (4)

$$t_1 = \frac{C_{LOAD1} V_{INIT}}{I_{INIT}} \quad (14)$$

Taking into account $T = t_1 + t_2 + t_3$, the capacitive load could be expressed

$$C_{LOAD1} = \frac{T}{\frac{V_{INIT}}{I_{INIT}} + \frac{1}{\alpha} \ln\left(\frac{V_{FIX} + \frac{I_{INIT}}{\alpha}}{V_{INIT} + \frac{I_{INIT}}{\alpha}}\right) + \frac{V_{OPER} - V_{FIX}}{I_{LIMIT}}} \quad (15)$$

The minimum value of C_{LOAD1} from equation (15) is obtained with T_{MIN}, V_{INIT_MAX}, I_{INIT_MIN}, and V_{FIX_MAX}. The same parametric limits must be used for expression of C_{NO_FLT} that follows.

Figure 2 shows this type of start-up transient.

The output voltage slew rate range for this case falls in the range:

$$S_{LOAD1\_MIN} = \frac{I_{INIT}}{C_{LOAD1}} \quad (15a)$$

$$S_{LOAD1\_MAX} = \frac{I_{LIMIT}}{C_{LOAD1}} \quad (15b)$$

Case 2: S_O Limits Current at Point A

For the case where the slew rate limit, S_O, causes the operating point to leave a current limit mode exactly at point A in Figure 1, the capacitive load C_{LOAD2} can be expressed as:

$$C_{LOAD2} \le \frac{I_{INIT} T}{V_{INIT}} \quad (16)$$

C_{LOAD2} has a minimum with I_{INIT_MIN}, T_{MIN} and V_{INIT_MAX}.

It should be noted that the maximum output voltage slew rate in this case is

$$S_{LOAD2\_MAX} = \frac{I_{INIT}}{C_{LOAD2}} \quad (16a)$$

It is constant while the operating point resides in the current limit mode.

Figure 3 shows this transient.

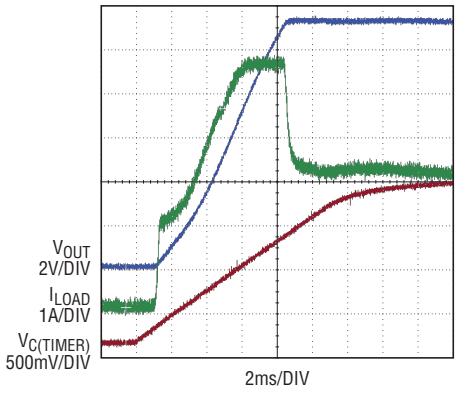


Figure 5. R-C load without limitation for S_O. Operating point leaves current limit mode in the third area, where current limit is I_{LIMIT}.

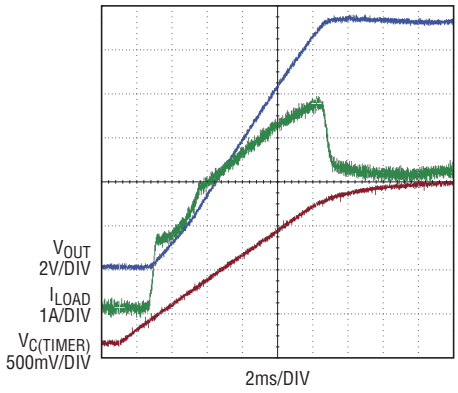


Figure 6. R-C load with limited S_O. Operating point leaves current limit mode in the first area, where current limit is I_{INIT}.

Case 3: S_O Limits Current at Point B

To produce an analytical expression of C_{LOAD3} for the case when the operating point leaves a current limit mode at point B, assume that it happens exactly as the output voltage reaches V_{FIX}. The full duration of operation in current limit mode, T, includes two intervals t_1 and t_2. According to (14) t_1 is:

$$t_{1\_3} = \frac{C_{LOAD3} V_{INIT}}{I_{INIT}} \quad (17)$$

In a second part of this transient, the output voltage changes according to expression (10) and the duration of interval t_2 is:

$$t_2 = \left(\frac{C_{LOAD3}}{\alpha}\right) \ln\left(\frac{V_{FIX} + \frac{I_{INIT}}{\alpha}}{V_{INIT} + \frac{I_{INIT}}{\alpha}}\right) \quad (18)$$

and from (17) and (18)

$$C_{LOAD3} = \frac{T}{\frac{V_{INIT}}{I_{INIT}} + \frac{1}{\alpha} \ln\left(\frac{V_{FIX} + \frac{I_{INIT}}{\alpha}}{V_{INIT} + \frac{I_{INIT}}{\alpha}}\right)} \quad (19)$$

From equation (19), the minimum value of C_{LOAD3} is produced using T_{MIN}, V_{INIT_MAX}, I_{INIT_MIN}, and V_{FIX_MAX}.

The output voltage slew rate range for this case can be defined as:

$$S_{LOAD3\_MIN} = \frac{I_{INIT}}{C_{LOAD3}} \quad (19a)$$

$$S_{LOAD3\_MAX} = \frac{I_{LIMIT}}{C_{LOAD3}} \quad (19b)$$

Case 4: S_O Limits Current Between Points A and B

If the output voltage slew rate S_O is in the range $S_{LOAD1\_MIN} \le S_O \le S_{LOAD1\_MAX}$, current limiting stops before the output voltage reaches V_{FIX} (before point B), meaning that during the time t_{1_4} the output voltage slew rate is a constant (due to I_{INIT}) and during the time t_{2_4} it becomes equal to S_O. The following method is recommended.

The output voltage rises from zero to the V_{FIX} during the time t_{1_4}, which can be expressed from (16) as

$$t_{1\_4} = \frac{C_{LOAD4} \bullet V_{INIT}}{I_{INIT}}$$

The output voltage $V_{OUT}(t_{2\_4})$ should be equal to the voltage on the second stage of the characteristic Figure 1 (equation 2):

$$V_{OUT}(t_{2\_4}) = \frac{I_{LOAD}(t_{2\_4}) - I_{INIT}}{\alpha} \quad (20)$$

Substituting $I_{LOAD}(t_{2\_4})$ in (14) with $S_O C_{LOAD4}$, taking into an account that $t_{2\_4} = T - t_{1\_4}$, and placing the equal sign between (14) and (11) forms the following equation:

$$\frac{S_O C_{LOAD4}}{\alpha} = \left(\frac{I_{INIT}}{\alpha} + V_{INIT}\right) e^{(\alpha t / C_{LOAD4})} \quad (21)$$

This transcendental equation (21) with unknown C_{LOAD4} can be solved with the proper calculation software (Mathcad, MATLAB, Mathematica) or LTspice.

Figure 4 demonstrates a successful power-up transient, where the current is limited for a time less than the timer period at maximum slew rate. As a result, the transient begins in current limit mode and finishes the inrush in slew rate limited operation.

The derived expressions in this article and the approach to the numerical solutions can serve as a basis for a detailed optimization of Hot Swap solutions.

MAXIMUM CAPACITIVE LOAD FOR SUCCESSFUL POWER-UP TRANSIENT WITHOUT THE LIMITATION OF THE OUTPUT VOLTAGE SLEW RATE AND A DEFINED RESISTIVE LOAD

If the passive load can be defined as a resistive load R_L and all Hot Swap circuit parameters (V_{OPER}, V_{FIX}, I_{INIT}, I_{LIMIT}, T) are known, then the maximum capacitive load should be found to ensure a successful power-up transient. A successful power-up transient is completed only after the current reaches I_{LIMIT}, because the slew rate is fast enough to stay in a current limit for the entire transient.

The differential equation for the first stage is:

$$C_{LR1}\frac{dV_{OUT}(t)}{dt}+\frac{V_{OUT}(t)}{R_L}=I_{INIT} \quad (22)$$

The equation (22) solution is:

$$V_{OUT}(t)=I_{INIT}\bullet R_L\left(1-e^{-t/C_{LR1}R_L}\right) \quad (23)$$

At the end of the first stage (t_1) the output voltage is equal to V_{INIT} and

$$t_1=C_{LR1}\bullet R_{LOAD}\bullet \ln\left(\frac{I_{INIT}\bullet R_L}{I_{INIT}\bullet R_L-V_{INIT}}\right) \quad (24)$$

The differential equation for the second stage is:

$$C_{LR1}\frac{dV_{OUT}(t)}{dt}+\frac{V_{OUT}(t)}{R_L}=I_{INIT}+\alpha V_{OUT}(t) \quad (25)$$

The first component on the left side of equation (25) is a current charging the capacitor; the second one is a resistive current.

The solution to equation (23) describes the output voltage from the beginning of this stage to the time t_2, when the output voltage reaches V_{FIX}.

$$V_{OUT}(t)=$$
$$=\left(V_{INIT}+\frac{I_{INIT}R_L}{\alpha R_L-1}\right)e^{\left(\frac{\alpha R_L-1}{C_{LR1}R_L}\right)t}-\left(\frac{I_{INIT}R_L}{\alpha R_L-1}\right)1 \quad (26)$$

The time interval t_2 could be expressed as a function of C_{LOAD} from (26) as:

$$t_2=\frac{R_LC_{LR1}}{\alpha R_L-1}\ln\left(\frac{V_{FIX}+\frac{I_{INIT}R_L}{\alpha R_L-1}}{V_{INIT}+\frac{I_{INIT}R_L}{\alpha R_L-1}}\right) \quad (27)$$

The differential equation for the third stage is:

$$C_{LR1}\frac{dV_{OUT}(t)}{dt}+\frac{V_{OUT}(t)}{R_L}=I_{LIMIT} \quad (28)$$

With the assumption that the output voltage slew rate, S_O, does not affect the transient, it is possible to say that the output voltage is changing according to (28) up to V_{OPER}. The solution for equation (28) is:

$$V_{OUT}(t)=$$
$$(V_{FIX}-I_{LIMIT}R_L)e^{(-t/C_{LR1}R_L)}+I_{LIMIT}R_L \quad (29)$$

At the end of this stage:

$$V_{OUT}(t_3)=V_{OPER}$$

And time t_3 equals:

$$t_3=R_LC_{LR1}\ln\left(\frac{V_{FIX}-I_{LIMIT}R_L}{V_{OPER}-I_{LIMIT}R_L}\right) \quad (30)$$

Since $T = t_1 + t_2 + t_3$, C_{LOAD} for this case is:

$$C_{LR1}=T\div\left\{\begin{array}{l}R_L\ln\left(\frac{I_{INIT}R_L}{I_{INIT}R_L-V_{INIT}}\right)+\\+\frac{R_L}{\alpha R_L-1}\ln\left(\frac{V_{FIX}+\frac{I_{INIT}R_L}{\alpha R_L-1}}{V_{INIT}+\frac{I_{INIT}R_L}{\alpha R_L-1}}\right)+\\+R_{LOAD}\ln\left(\frac{V_{FIX}-I_{LIMIT}R_L}{V_{OPER}-I_{LIMIT}R_L}\right)\end{array}\right\} \quad (31)$$

Figure 5 shows measured results for this case.

MAXIMUM CAPACITIVE LOAD FOR SUCCESSFUL POWER-UP TRANSIENT WHEN CURRENT IS LIMITED BY THE OUTPUT VOLTAGE SLEW RATE AND A DEFINED RESISTIVE LOAD IS PRESENT

The value of the output voltage slew rate, S_O, defines how long a Hot Swap circuit should operate in the current limit mode. This event (leaving the current limit mode) can happen at any moment of the three stages of the transient. For defined points A and B, during the third stage it is possible to use equations from the previous section. For any intermediate points, it is possible to use the approach demonstrated in "Case 4" with a transcendental equation.

The transient in Figure 6 illustrates this case, when the operating point leaves the current limit mode in the first stage of current limit area.

CONCLUSION

The derived expressions in this article and the approach to the numerical solutions can serve as a basis for a detailed optimization of Hot Swap solutions. ■

New Product Briefs

0V TO 100V, 1% ACCURATE ENERGY MONITOR HAS 12-BIT OUTPUT

The LTC2946 is a high or low side charge, power and energy monitor for DC supply rails in the 0V to 100V range. An integrated ±0.4% accurate, 12-bit ADC and external precision time base (crystal or clock) enables measurement accuracy better than ±0.6% for current and charge, and ±1% for power and energy. A ±5% accurate internal time base substitutes in the absence of an external one. All digital readings, including minimums and maximums of voltage, current and power, are stored in registers accessible by an I²C/SMBus interface. An alert output signals when measurements exceed configurable warning thresholds, relieving the host of burdensome polling for data. The LTC2946 provides access to all the necessary parameters to accurately assess and manage board level energy consumption.

The LTC2946 can be powered from 2.7V to 5V directly, from 4V to 100V through an internal linear regulator, or beyond 100V through an internal shunt regulator. Two of the three general purpose input/output (GPIO) pins are configurable as an accumulator enable and alert output. The internal ADC operates in either a continuous scan mode or a snapshot mode. In shutdown mode, the device current consumption drops from 900µA to 15µA.

The LTC2946 is offered in 16-pin MSOP and 4mm × 3mm DFN packages.

4µA I_Q Hot Swap CONTROLLER PROTECTS BATTERIES FROM VOLTAGE & CURRENT FAULTS

The LTC4231 is an ultralow quiescent current (I_Q) Hot Swap controller, enabling safe board or battery insertion and extraction from 2.7V to 36V systems. The LTC4231 controls an external N-channel MOSFET to gently power-up board capacitors, avoiding sparks, connector damage and system glitches. Device quiescent current is a mere 4µA during normal operation, dropping to 0.3µA in shutdown mode. To ensure low current operation, the undervoltage and overvoltage resistive dividers are connected to a strobed ground, lowering their average current draw by 50×. The LTC4231 provides a compact and rugged micropower solution for hot plugging and battery protection, especially in energy conscious applications utilizing solar power or energy harvesting.

The LTC4231 survives and also protects downstream circuitry from reversed batteries up to –40V by controlling back-to-back N-channel MOSFETs. Undervoltage protection cuts off low voltage batteries to prevent deep discharge, while adjustable hysteresis avoids oscillations from battery recovery after load removal. Dual level overcurrent protection is provided by a timed circuit breaker and fast current limit. The 2.7V to 36V operating range accommodates a wide range of battery chemistries including lead-acid, Li-ion and stacked NiCd.

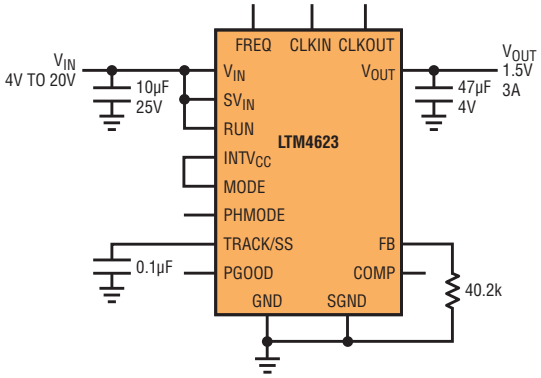
The LTC4231 is offered in 12-pin MSOP and 3mm × 3mm QFN packages.

36V MONOLITHIC 1A PUSH-PULL DC/DC TRANSFORMER DRIVER WITH PROGRAMMABLE DUTY CYCLE CONTROL

The LT3999 is a monolithic push-pull isolated DC/DC transformer driver with two 1A current limited power switches. The LT3999 operates over an input voltage range of 2.7V to 36V, is targeted for power levels up to 15W and can produce a wide range of output voltages. This makes it well suited for automotive, industrial, medical and military applications.

The programmable duty cycle and turns ratio of the transformer sets the output voltage. Several off-the-shelf transformers shown in the data sheet simplify the design. The switching frequency is adjustable from 50kHz to 1MHz and can be synchronized to an external clock. The LT3999 input operating voltage range is set with the precise undervoltage and overvoltage lockouts. The supply current is reduced to less than 1µA during shutdown. A user-defined RC time constant provides an adjustable soft-start capability by limiting the inrush current at start-up and an onboard cross-conduction prevention circuit increases reliability.

The LT3999 is available in thermally enhanced MSOP-10 and 3mm × 3mm DFN-10 packages. ■



LTM4623 4V–20V V_{IN}, 1.5V V_{IN} AT 3A WITH ULTRALOW PROFILE (< 2mm)

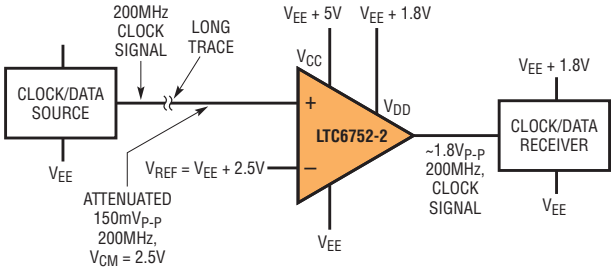
The LTM4623 is a complete 3A step-down switching mode µModule (micromodule) regulator in an ultrathin 6.25mm × 6.25mm × 1.82mm LGA package. Included in the package are the switching controller, power FETs, inductor and support components. Operating over an input voltage range of 4V to 20V or 2.375V to 20V with an external bias supply, the LTM4623 supports an output voltage range of 0.6V to 5.5V, set by a single external resistor. Its high efficiency design delivers 3A continuous output current. Only ceramic input and output capacitors are needed.

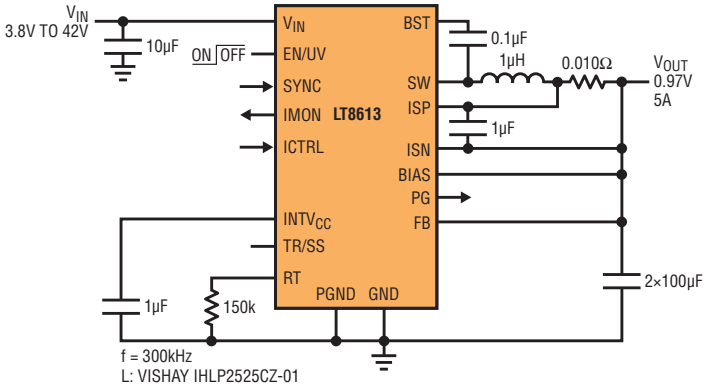
www.linear.com/solutions/5527

LTC6752 200MHz CLOCK RESTORATION/LEVEL SHIFTING

High speed comparators are often used in digital systems to recover distorted clock waveforms. The LTC6752-2 features independent input and output supplies, allowing it to be used in applications where signals must be shifted from one voltage domain to another. This circuit can perform both recovery and level translation functions. In this application, the input clock signal is from a source operating from 5V, with a receiver operating on 1.8V. The 5V input supply/1.8V output supply feature of he LTC6752-2 is ideal for such a situation. If the input signal is distorted and its amplitude severely reduced due to stray capacitance, stray inductance or reflections on the transmission line, the LTC6752-2 can convert it into a full scale digital output signal suitable for driving the receiver.

www.linear.com/solutions/5530





LT8613 1V STEP-DOWN WITH 5A OUTPUT CURRENT LIMIT

The LT8613 is a compact, high efficiency, high speed synchronous monolithic step-down switching regulator that consumes only 3µA of quiescent current. Top and bottom power switches are included with all necessary circuitry, minimizing the need for external components. The built-in current sense amplifier with monitor and control pins allows accurate input or output current regulation and limiting. Low ripple Burst Mode operation enables high efficiency down to very low output currents while keeping the output ripple below 10mV$_{P-P}$. A SYNC pin allows synchronization to an external clock. Internal compensation with peak current mode topology allows the use of small inductors and results in fast transient response and good loop stability. The EN/UV pin has an accurate 1V threshold and can be used to program V_{IN} undervoltage lockout or to shut down the LT8613, reducing the input supply current to 1µA. A capacitor on the TR/SS pin programs the output voltage ramp rate during start-up. The PG flag signals when V_{OUT} is within ±9% of the programmed output voltage as well as fault conditions. The LT8613 is available in a small 28-lead 3mm × 6mm QFN package with exposed pad for low thermal resistance.

www.linear.com/solutions/5543

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